

MODEL NAME : BAP10(15")/BAP20(17")
PROJECT CODE : ANRBAP1000/ANRBAP2000
PCB NO :
DAC00004000 LA-D751P M/B(NV)
DAC00005000 LA-D751P M/B(NV_G3)
DA4002AV000 LS-D751P LOGO_15/B
DA80017I000 LS-D752P LOGO_17/B
DA4002B000S LS-D753P PWR_15/B
DA4002AW000 LS-D754P PWR_17/B
DA80017J000 LS-D755P IO_12L/B
DA4002AY000 LS-D757P TRON_LCD_15/B
DA4002AZ000 LS-D758P TRON_REAR_15/B
DA80017K000 LS-D759P IO_14L/B
DA4002D4000 LS-D75AP TRON_LCD_17/B
DA4002D5000 LS-D75BP TRON_REAR_17/B
DA4002D7000 LS-D75CP TRON_FRONT_15/B
DA4002D8000 LS-D75DP TRON_FRONT_17/B
DA30000W300 LF-D751P Head_15/B
DA30000W400 LF-D752P Head_17/B
DA30000W401 LF-D752P Head_17/B(For LOGO_15/B)
DA30000SY00 LF-D753P TRON_15/B
DA30000WX00 LF-D754P TRON_17/B

ZZZ PCB@
PCB 1JM LA-D751P REV0 MB NV 16
DAC00004000

ZZZ PCBR1@
PCB 1JM LA-D751P REV1 MB NV 16
DAC00004010


ZZZ PCBR3@
PCB 1JM LA-D751P REV1 MB NV TRIP 16 A31!
DAC00004011

ZZZ DAZR1@
PCB BAP10 LA-D751P LS-D751P-2P/D754P/D757P-DP 02
DAZ1JM00100

ZZZ DAZR3@
PCB BAP10 LA-D751P LS-D751P-2P/D754P/D757P-DP 02 TRI A31 !
DAZ1JM00101

HDMI@ ROYALTY HDMI W/LOGO	
Part Number	Description
RO00000003RM	HDMI W/Logo:RO0000003RM

Layout Dell logo



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REV: X00
PWB: XXXXX
DATE: 1450-06

BAP10/BAP20 Skylake/Kabylake-H 45W

Skylake/Kabylake PCH with nVidia N17P/N17E

REV : 1.0 (A00)

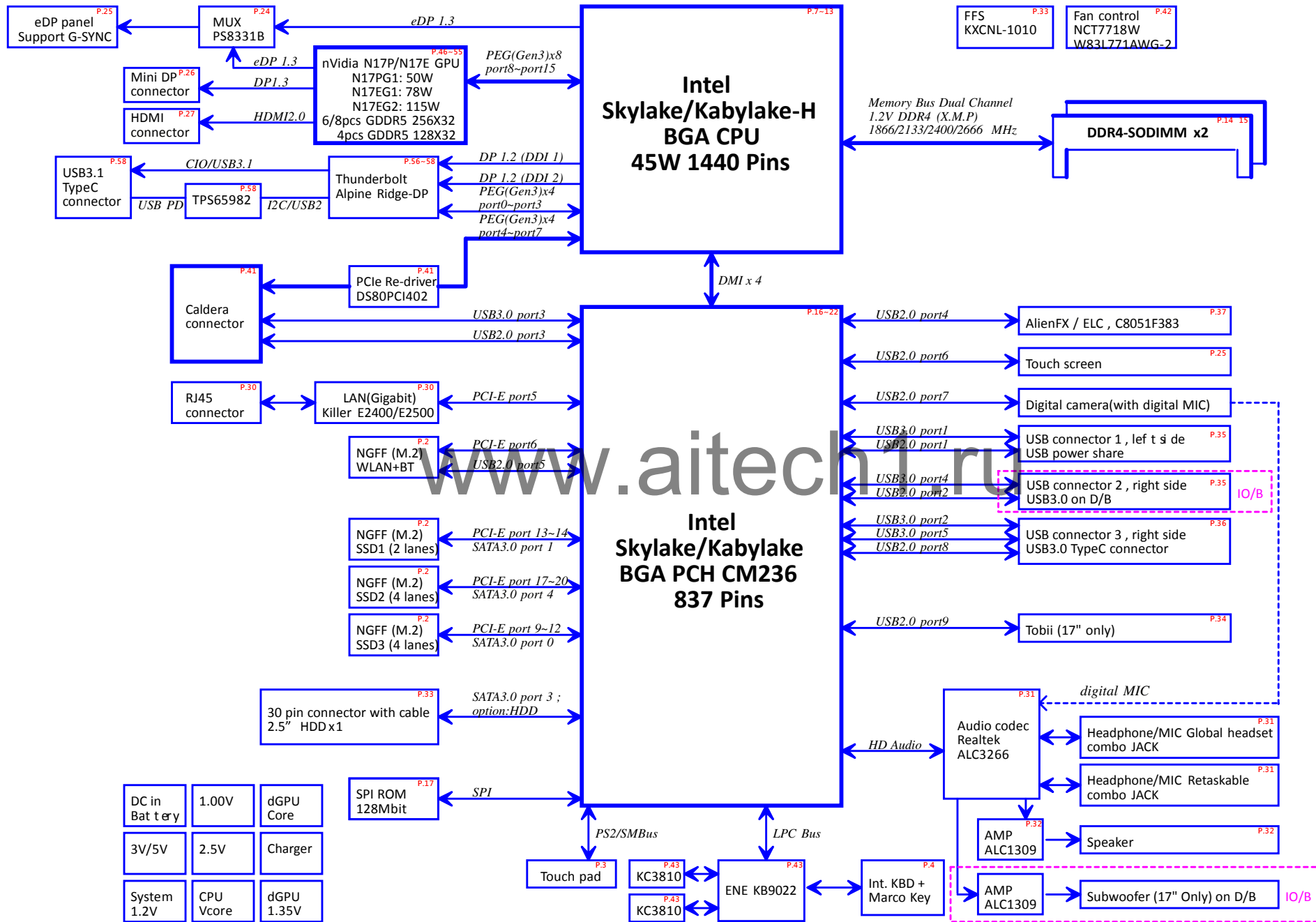
2016.08.15

@ : Nopop Component
EMI@,ESD@,RF@ : EMI/ESD/RF part

CONN@ : Connector Component
@EMI@,@ESD@,@RF@ : Total debug Component

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				Date:	Rev
				Friday, August 19, 2016	LA-D751P
				Sheet	1.0
				1	82

Block Diagram

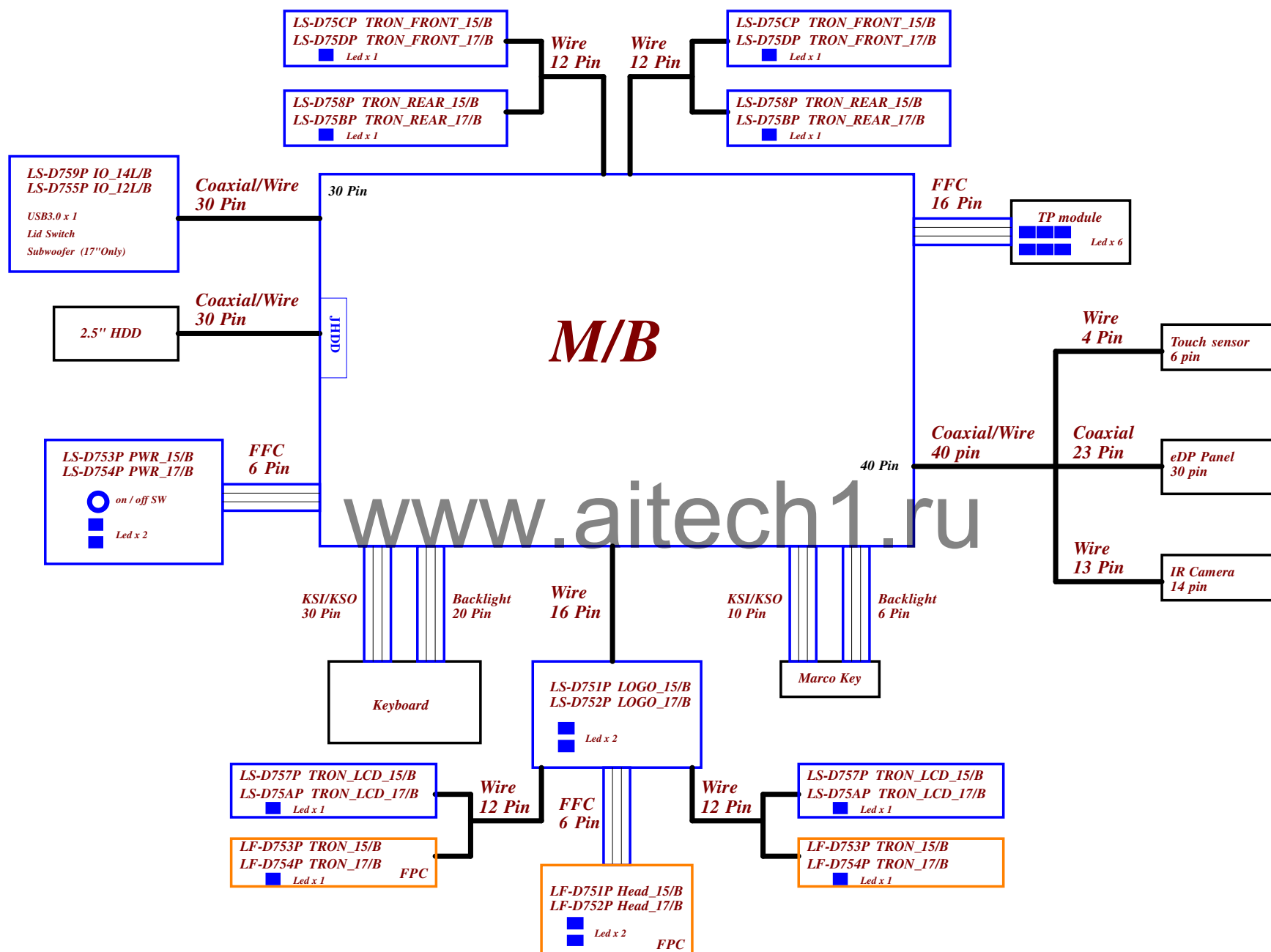


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PCB

FPC

Module



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Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x13
1	12K +/- 1%	0.347V	0.354V	0.360V	0x14 - 0x1E
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1F - 0x25
3	20K +/- 1%	0.541V	0.550V	0.559V	0x26 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3A
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3B - 0x45
6	43K +/- 1%	0.978V	0.992V	1.006V	0x46 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA4
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA5 - 0xAF
13	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xBF
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC0 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD4
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD5 - 0xDD
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDE - 0xF0
19	NC	3.000V	3.300V	3.300V	0xF1 - 0xFF

Voltage Rails

Power Plane	Description	S0	S3	S4 / S5
VIN	Adapter power supply	N/A	N/A	N/A
BATT+	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF
+1VALW	System +1VALW power rail	ON	ON	ON*
+1V_PRIM	System +1VALW power rail	ON	ON	ON*
+VCCIO	+1.0VS IO power rail	ON	OFF	OFF
+VGA_PCIE	+1.0VS power rail for GPU	ON	OFF	OFF
+MEM_GFX	+1.5VS power rail for GPU	ON	OFF	OFF
+1.2V_VDDQ	DDR-IV +1.2V power rail	ON	ON	OFF
+1VS_VCCST	+1.0V power rail for CPU	ON	ON	OFF
+1VS_VCCSTG	+1.0VS power rail for CPU	ON	OFF	OFF
+3VALW	System +3VALW always on power rail	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON*
+3V_LAN	+3VALW power for LAN power rails	ON	ON	ON*
+3VS	System +3VS power rail	ON	OFF	OFF
+1.8VS	+1.8VS power rail for GPU	ON	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON*
+5VS	System +5VS power rail	ON	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON
+VCC_SA	System Agent power rail	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

Board ID TABLE

SKL ID	PCB Revision
NV	
0	EVT
1	DVT-1
2	DVT-1.1
3	DVT-2 / DVT-2.1
4	GC6
5	Pilot build

KBL ID	PCB Revision
NV	
1	EVT
6	DVT-1 / DVT-1.1
7	GC6
8	DVT-2
9	Pilot build

PCH-H CM236

HSIO	USB3	PCIe	SATA3	Function
1	1			JUSB1,type A
2	2			JUSBC2,type C
3	3			Caldera
4	4			JIO,IO/B
5	5			JUSBC2,type C
6	6			
7	7	1		
8	8	2		
9	9	3		
10	10	4		
11		5		LAN
12		6		WLAN
13		7		
14		8		
15		9	0	JSSD3 M.2 2280 SATA PCIe x4
16		10	1	
17		11		
18		12		
22		16	3	JSSD5/HDD SATA
21		15		
20		14	1	JSSD1 SATA/PCIe x2
19		13	0	
23		17	4	
24		18	5	JSSD2 M.2 2280 SATA PCIe x4
25		19		
26		20		

* PCIe 13~16 in "Lane Reversal Mode". (HSIO Port 19~22)

USB2	Function
1	JUSB1(Powershare)
2	JIO(IO/B)
3	Caldera
4	ELC
5	Bluetooth
6	Touch screen
7	Camera
8	JUSBC2
9	Tobii
10	
11	
12	
13	
14	

Symbol Note :



Digital Ground



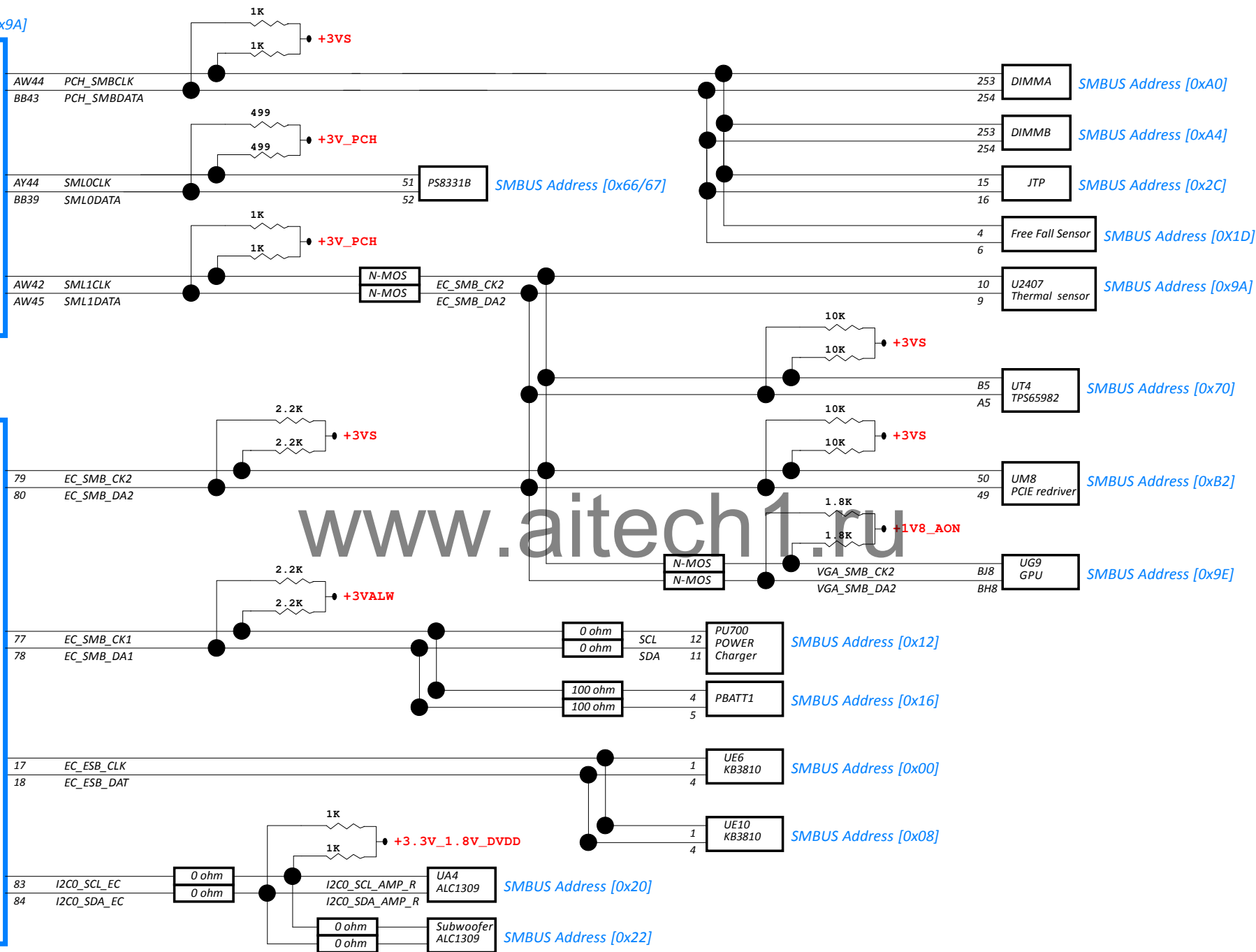
Analog Ground

CPU,C
DDR,D
GPU,DP,HDMI,EDP,V
LAN,L
AUDIO,A
NGFF,N
USB,U
CALDERA,M
HDD,S
ELC,E
FAN,F
TP,T
KBC,K
DC,O

SMBUS Address [0x9A]

Kaby Lake
PCH-H

KBC
KB9022QD

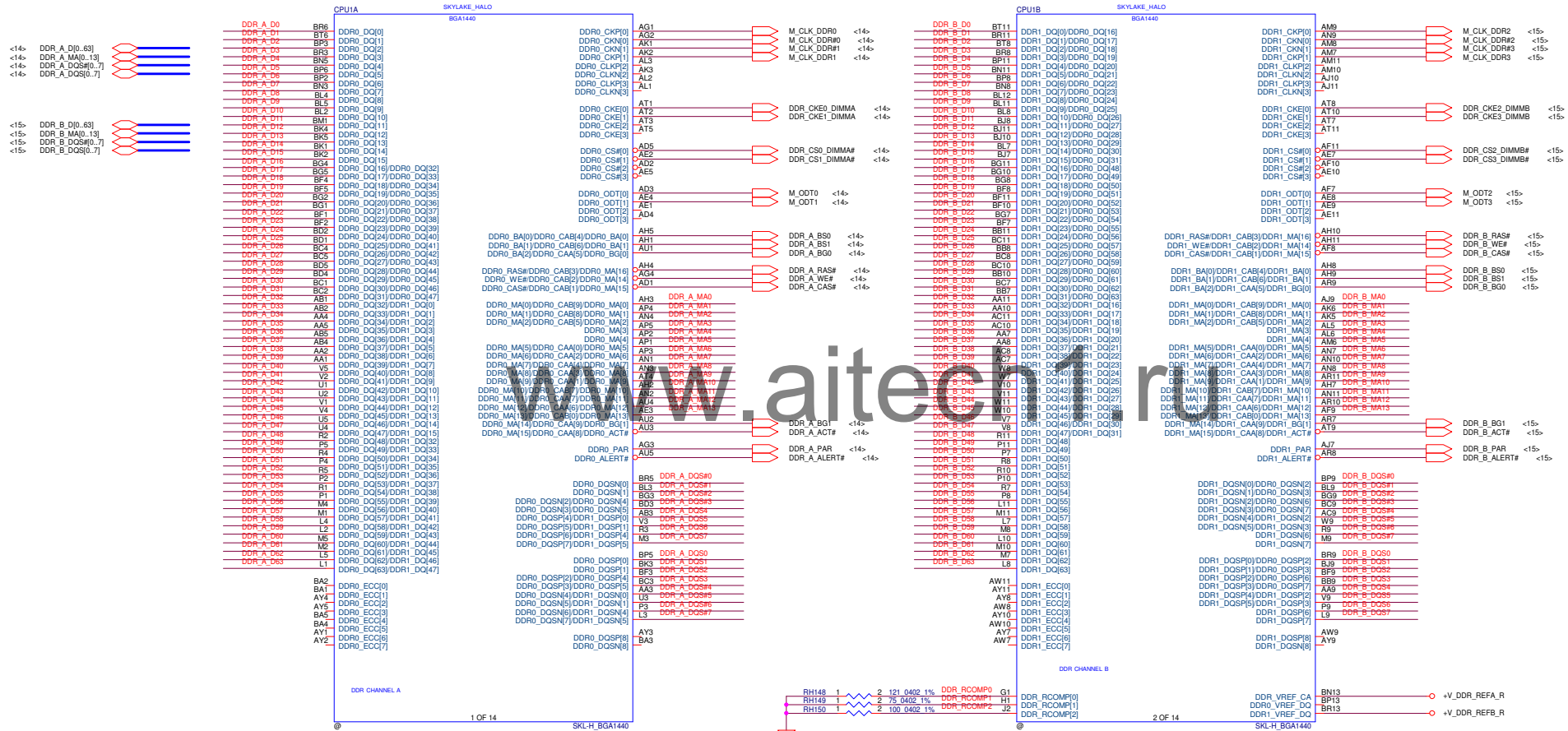


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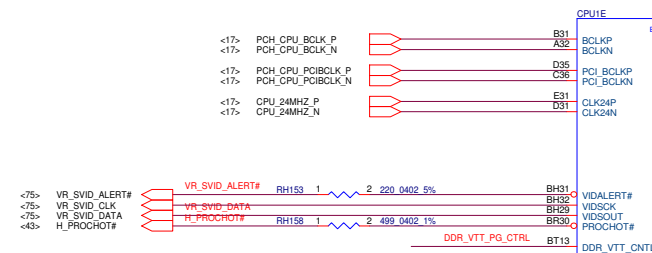
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Interleave



DDR_RCOMP0 :
DDR_RCOMP1 :
DDR_RCOMP2 :
Trace width=12~15 mils
Spacing=20 mils
Max length= 500 mils

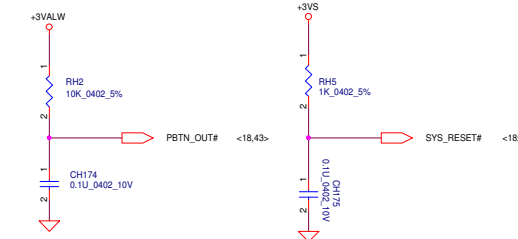
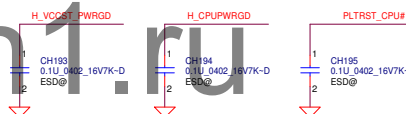
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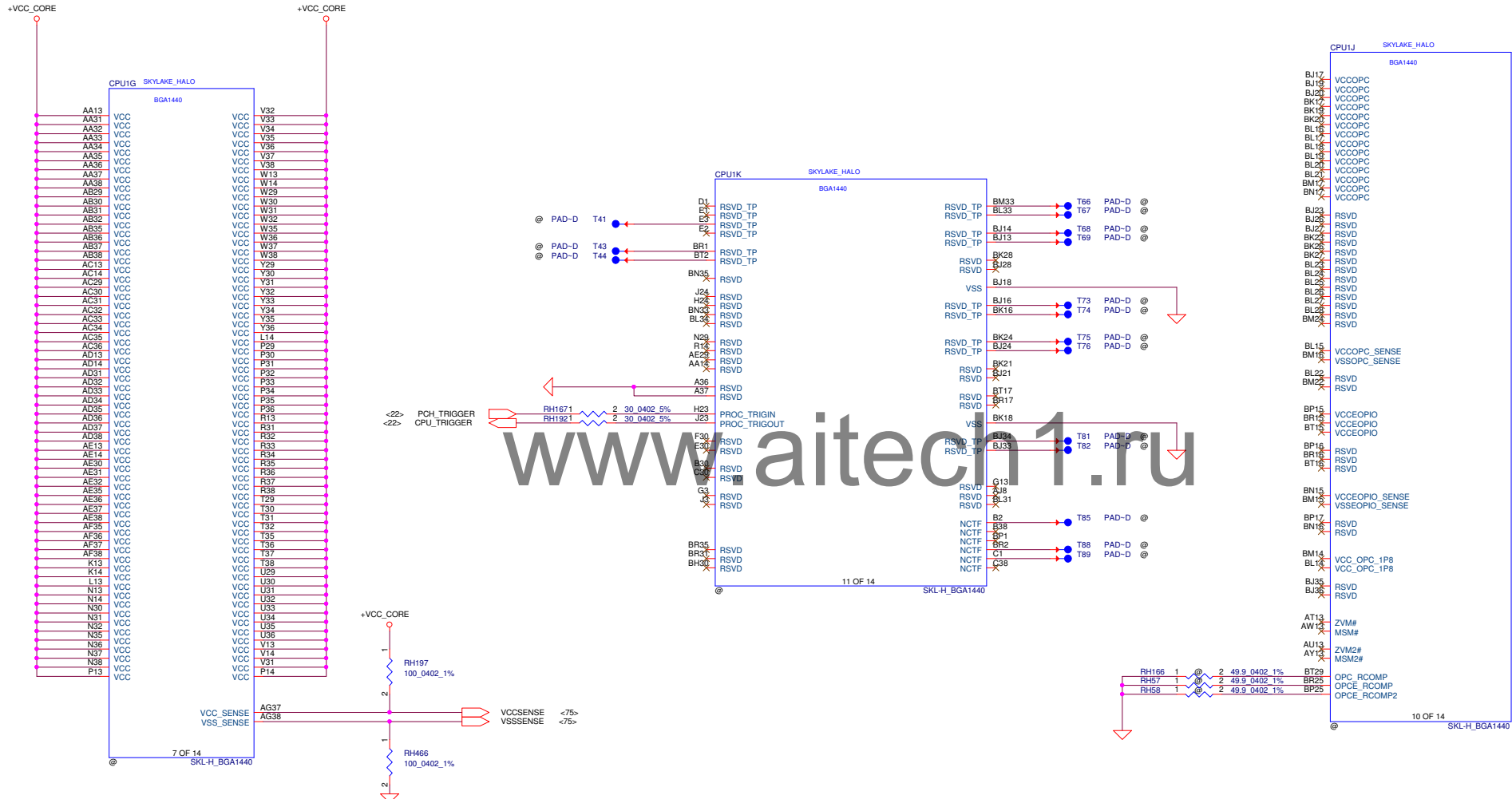


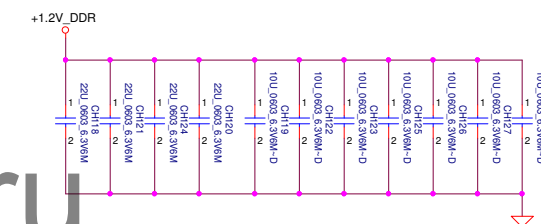
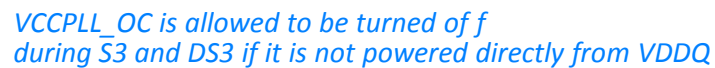
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RH186 1K_0402_5%

CFG6 1 2
RH187 1K_0402_5%

CFG7 1 2
RH188 1K_0402_5%

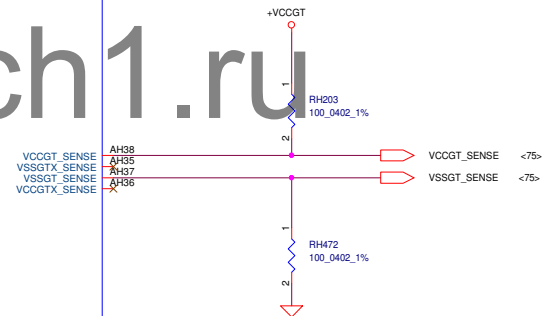
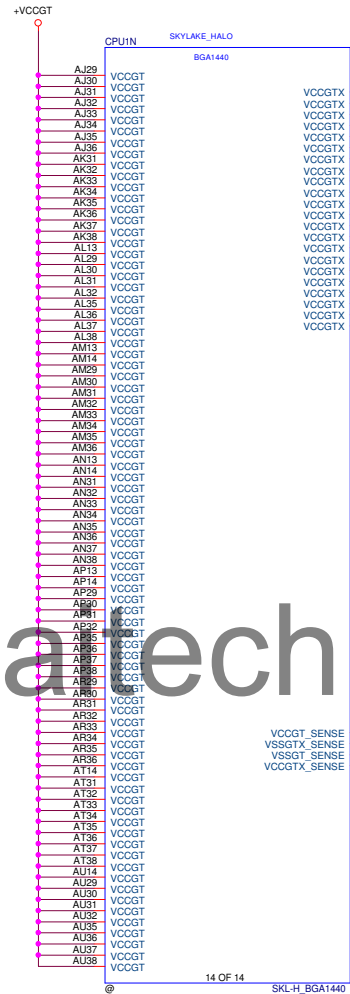
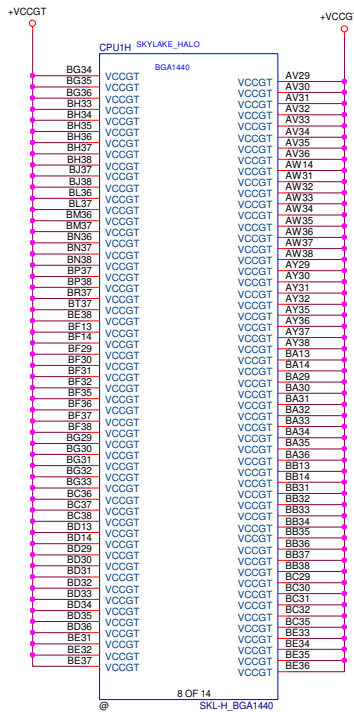




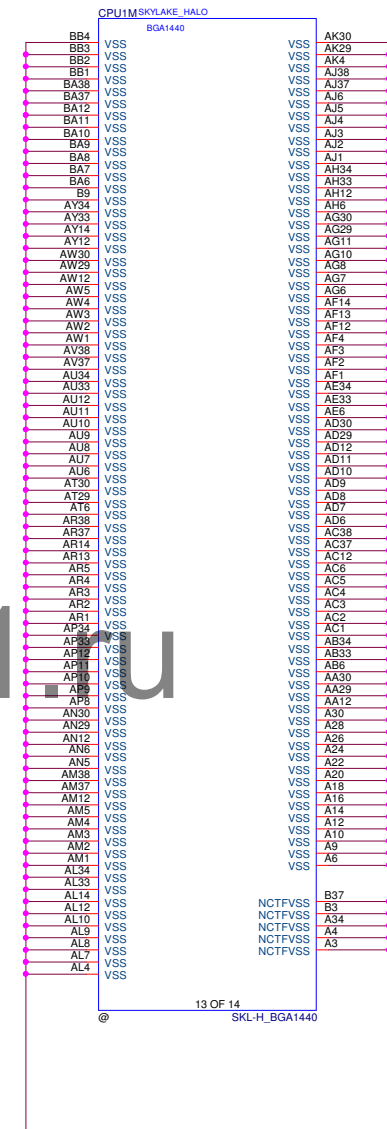
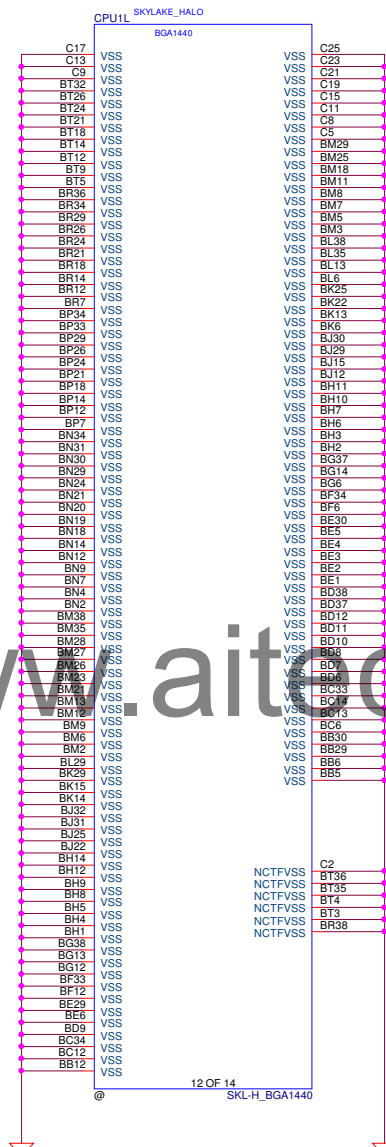
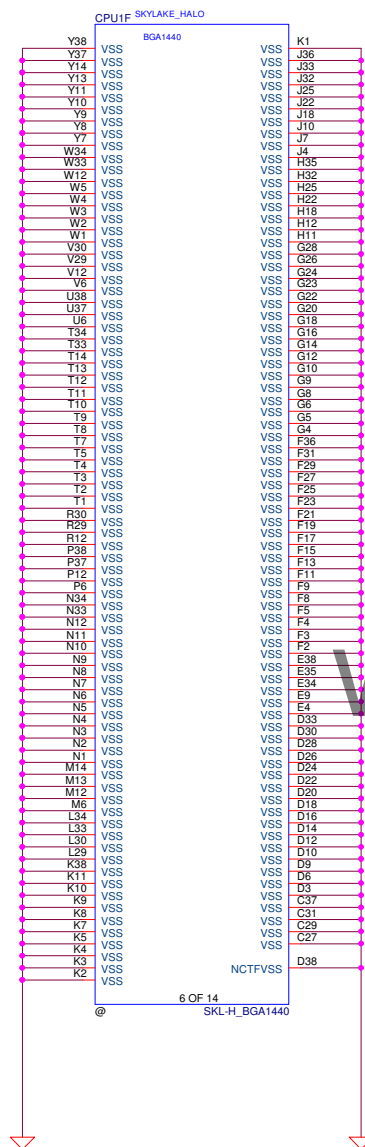


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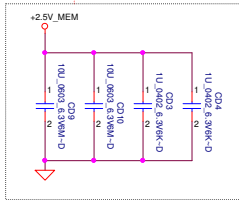


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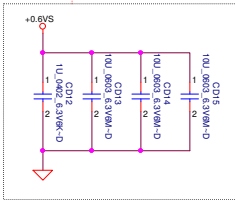


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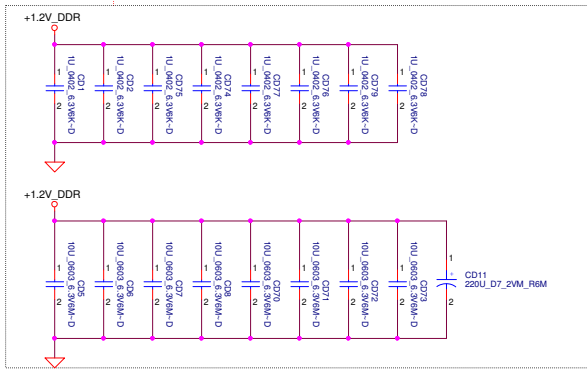
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Layout Note:
Place near JDIMM1.258



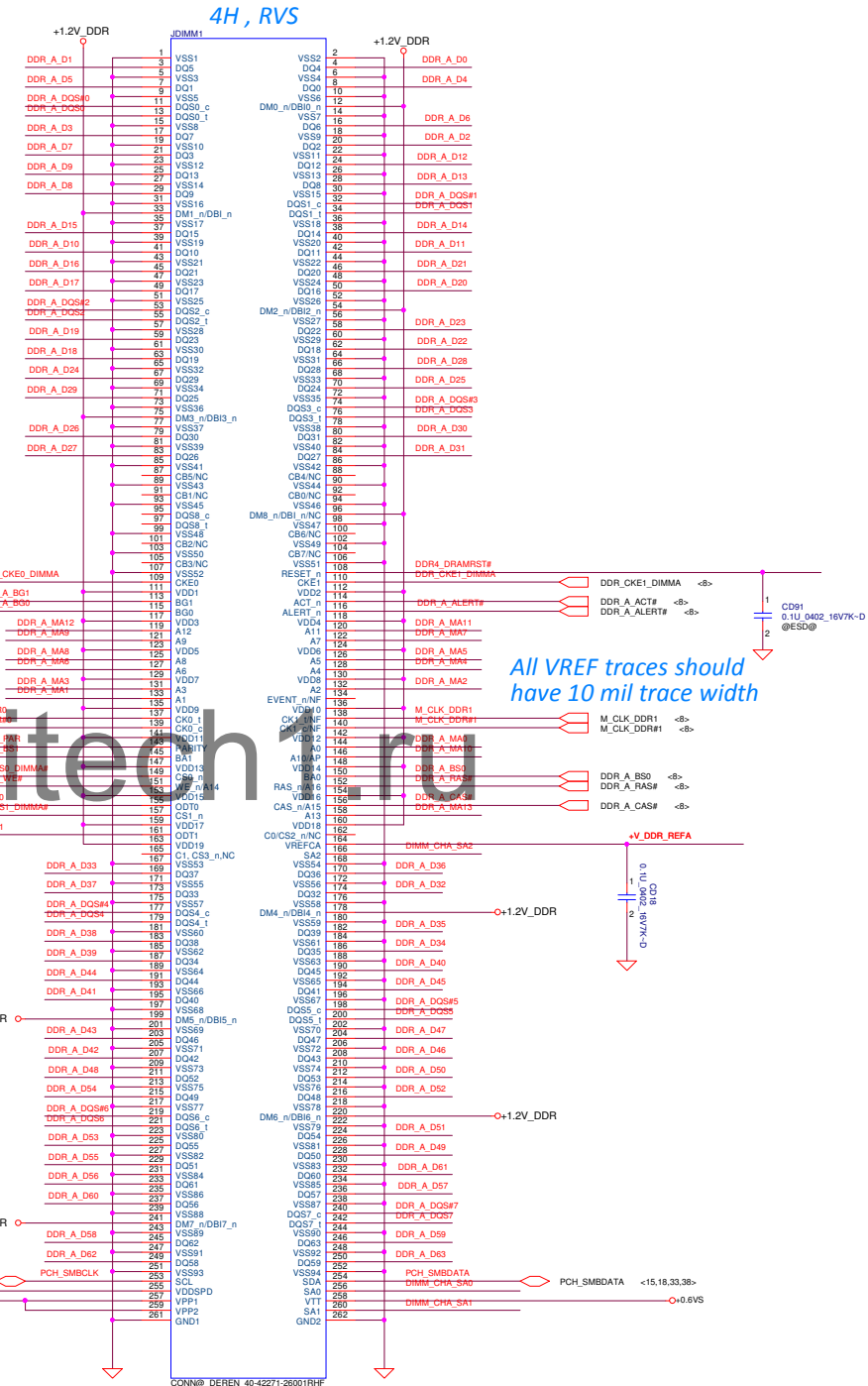
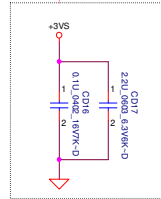
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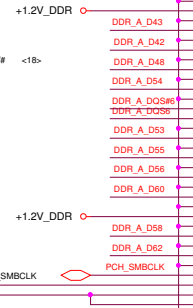
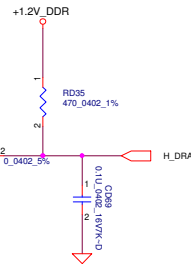
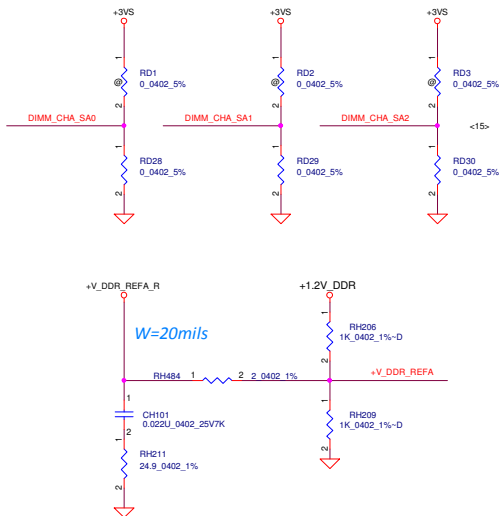
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 DDR_A_DQS[0..7]
 DDR_A_DQS[0..7]

CFG Straps for Processor

Layout Note:
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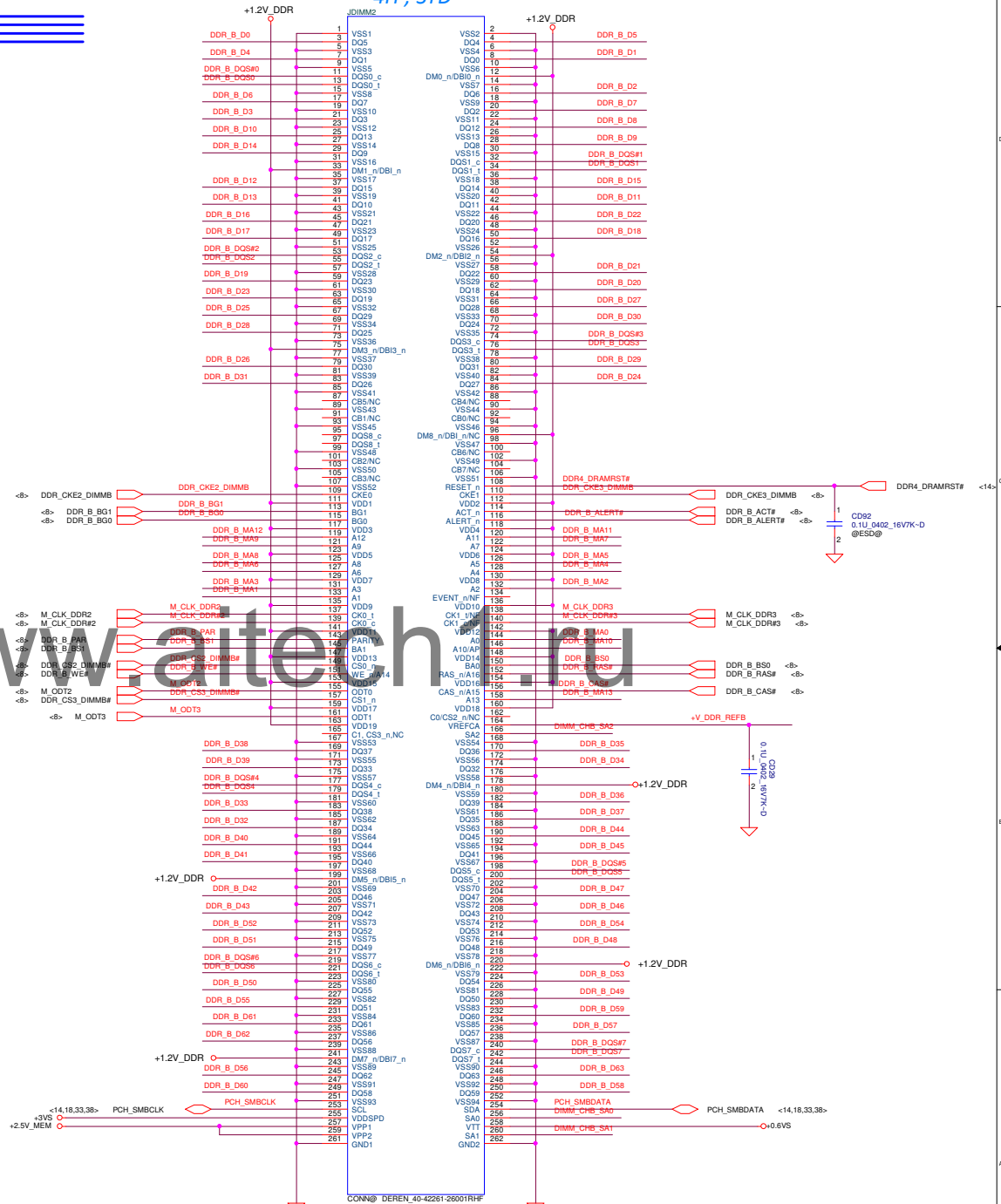
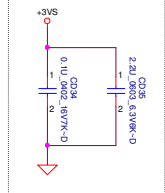
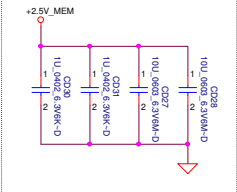
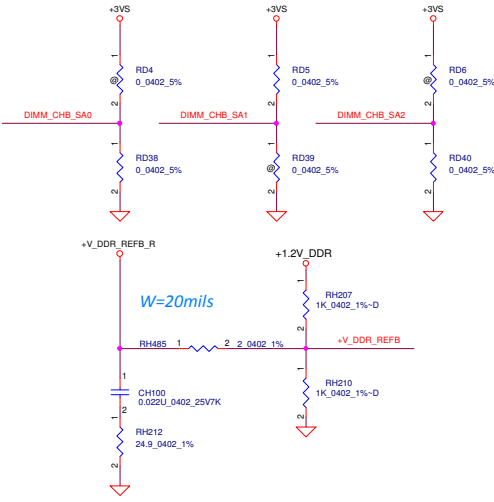


All VREF traces should
have 10 mil trace width



CONN@ DEREN_40-42271-26001RHF

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S IC GLCM236 SR2CE D1 FCBGA 837P PCH-H
SA00009601L
PCHR1@

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SA00009602L
PCHR3@

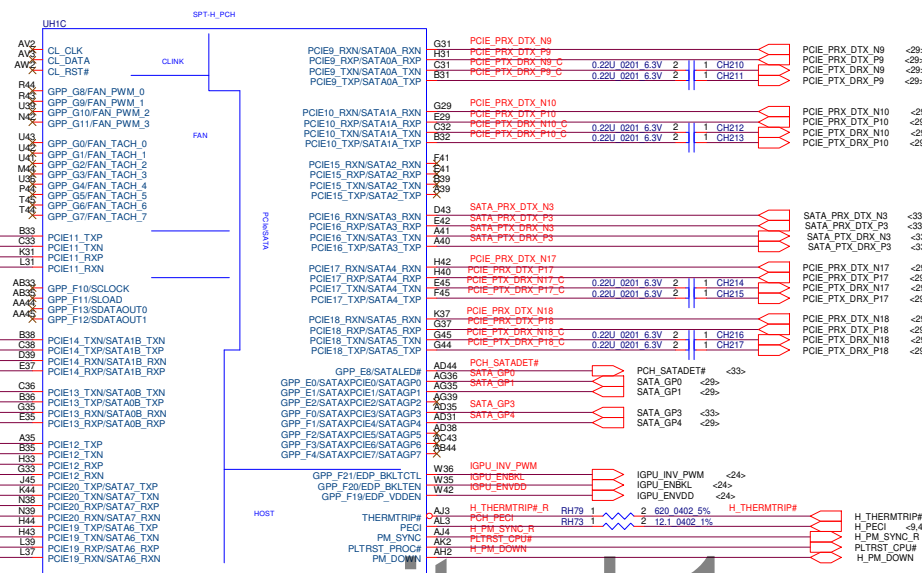
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PCHES@

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PCIe/SATA

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PCIe/SATA

M.2 SSD Slot#3
PCIe/SATA

M.2 SSD Slot#2
PCIe/SATA

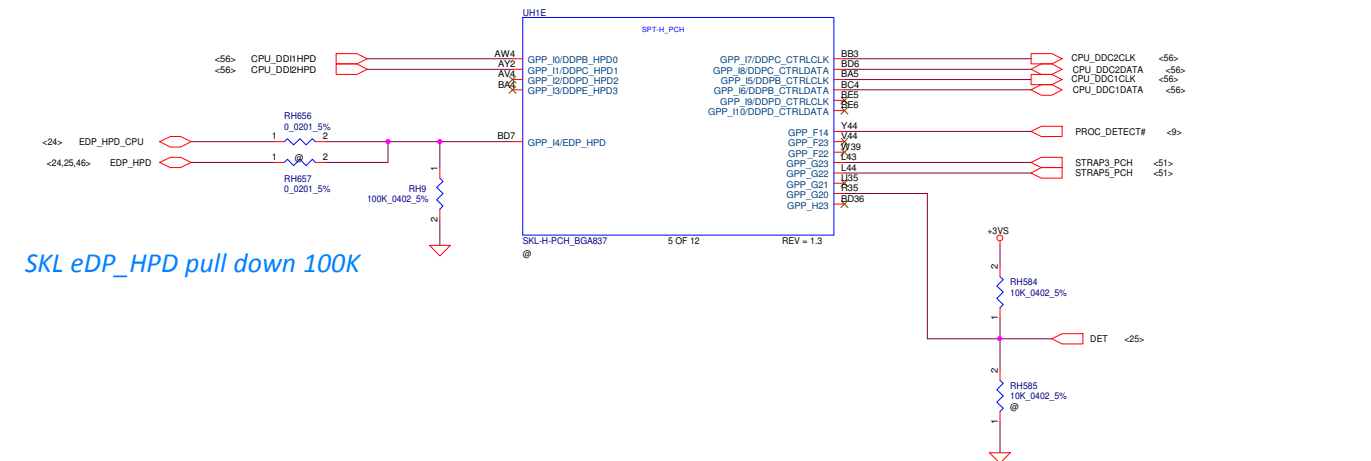


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PCIe/SATA

M.2 SSD Slot#5
or SATA HDD

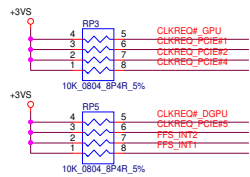
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PCIe/SATA

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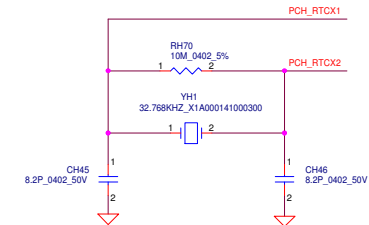
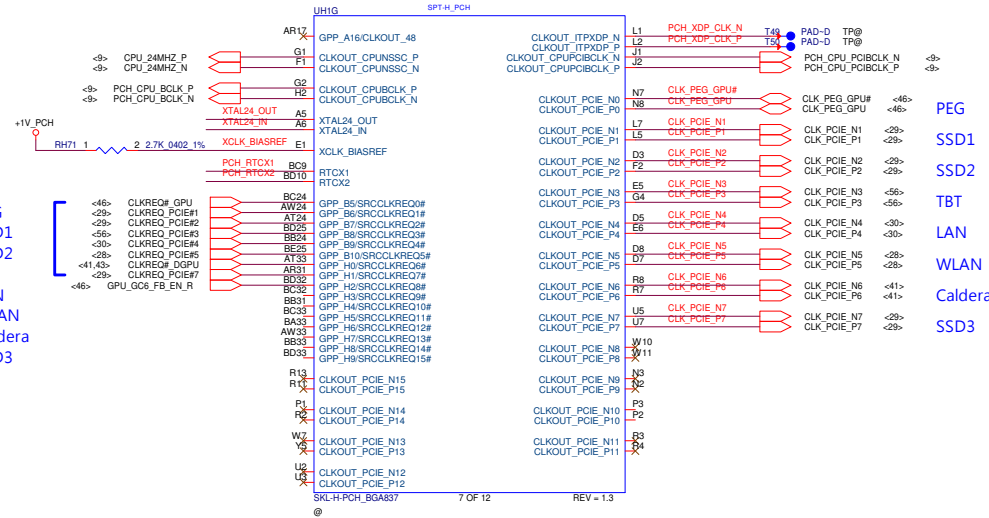


SKL eDP_HP pull down 100K

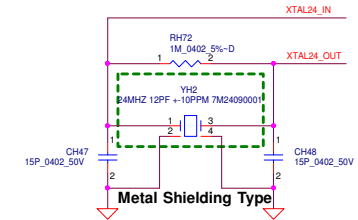
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Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title
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Size	Document Number	Rev	1.0	Rev
LA-D751P	LA-D751P	1.0	1.0	1.0
Date:	Tuesday, August 16, 2016	Sheet	16	of 82



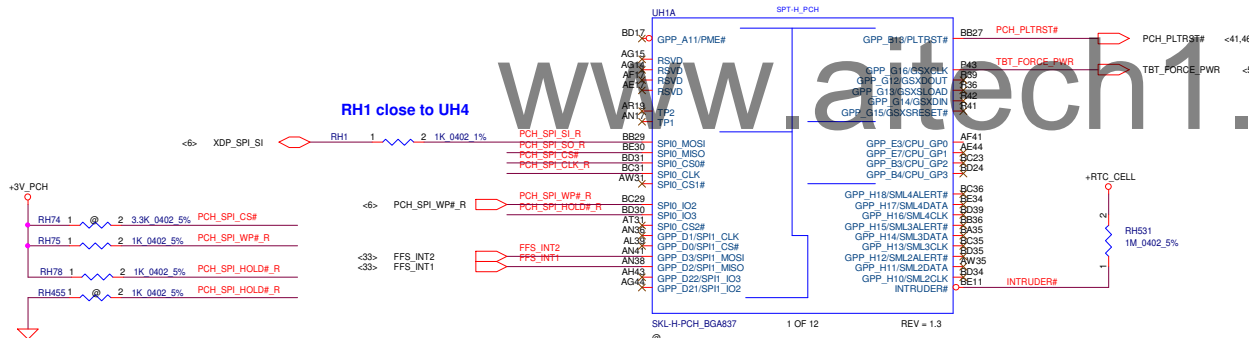
- 0. PEG
- 1. SSD1
- 2. SSD2
- 3. TBT
- 4. LAN
- 5. WLAN
- 6. Caldera
- 7. SSD3



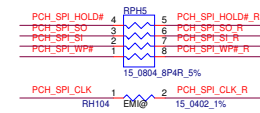
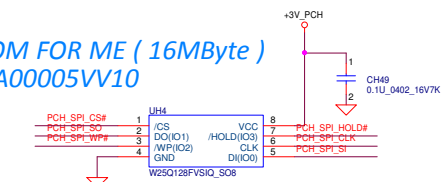
RTC CRYSTAL
Max Crystal ESR
= 50k Ohm.



Metal Shielding Type

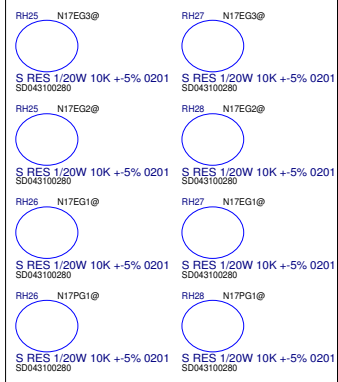
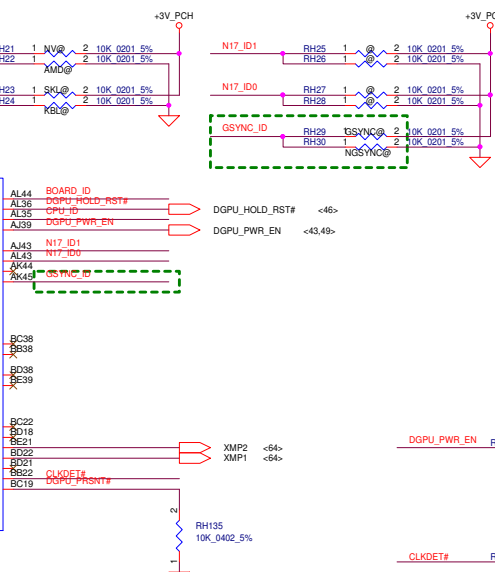
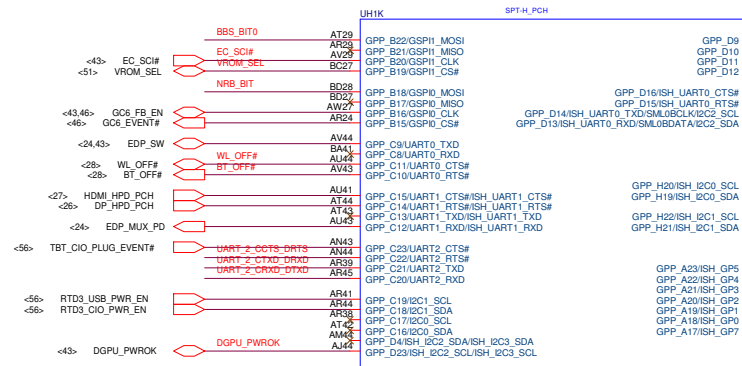
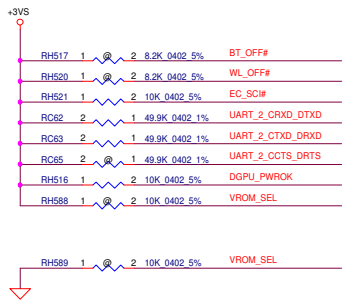


SPI ROM FOR ME (16MByte)
PN: SA00005VV10



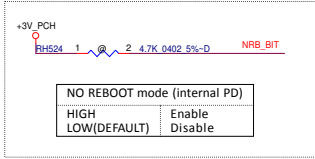
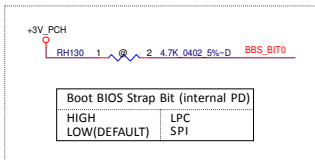
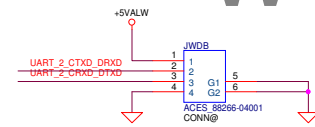
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Issued Date	2016/01/06	Deciphered Date	2017/01/06
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		Size	17 of 82
		Date	Tuesday, August 16, 2016
		Sheet	17 of 82
		Rev	1.0

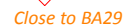




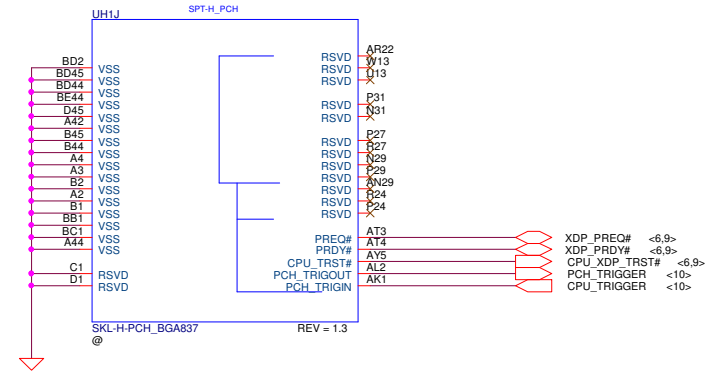
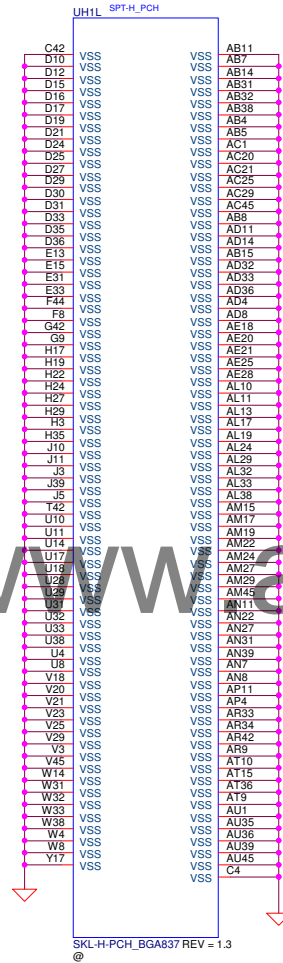
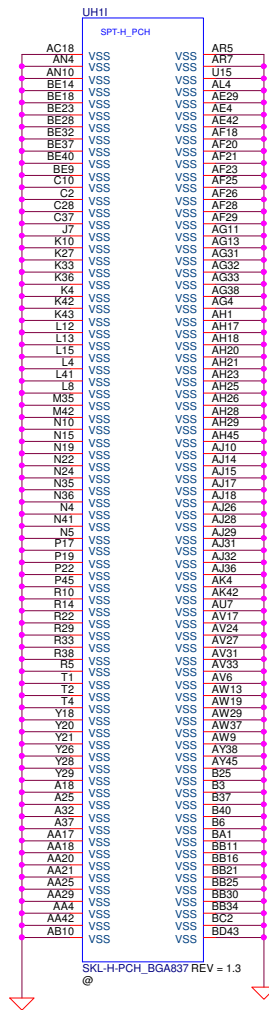
nVidia GPU_ID	N17_ID1	N17_ID0
N17EG3	H	H
N17EG2	H	L
N17EG1	L	H
N17PG1	L	L

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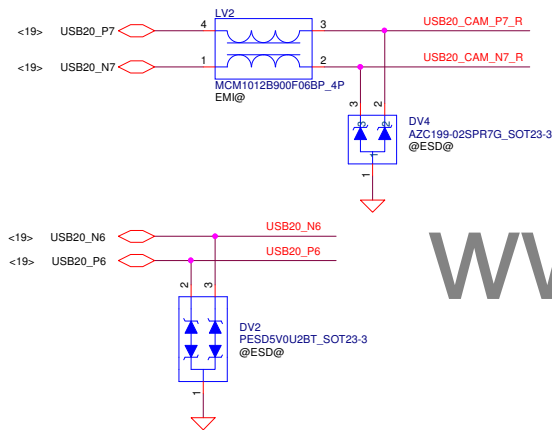
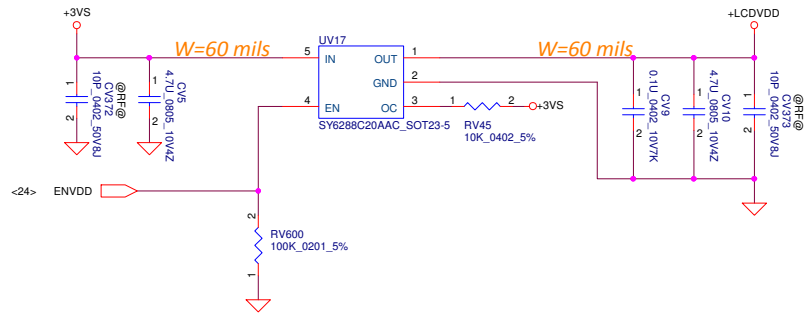


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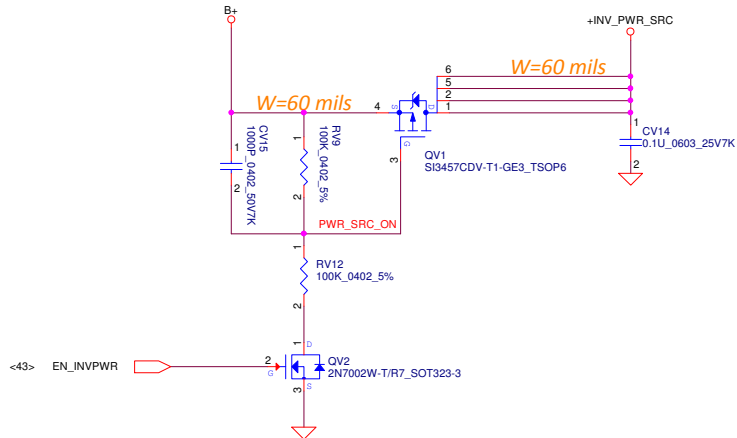
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				Size	Document Number
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LCD power control

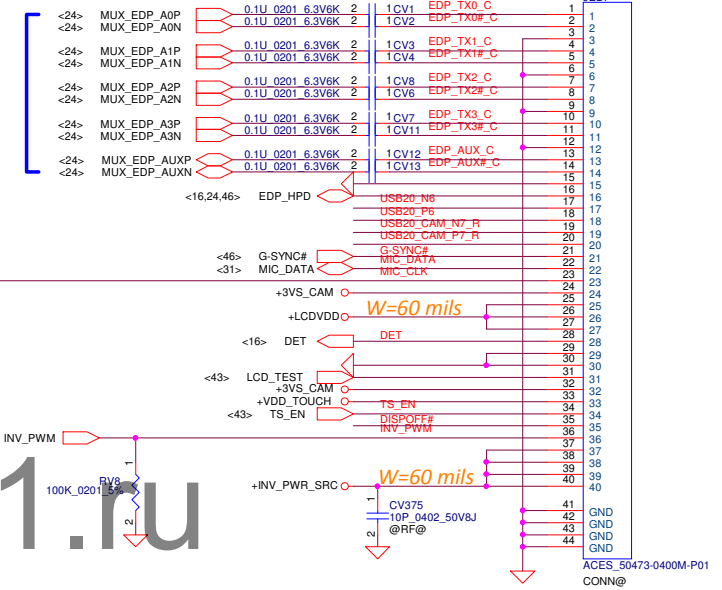


LCD backlight power control



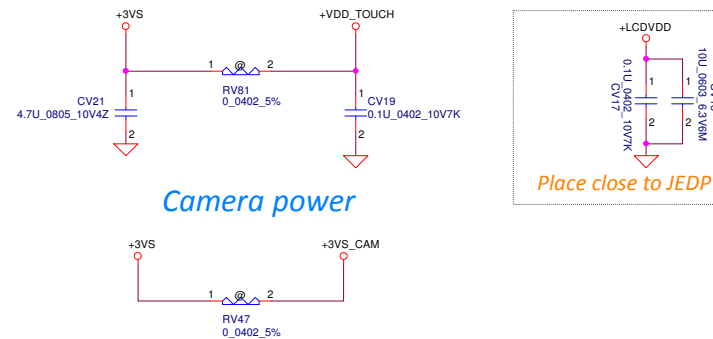
From eDP MUX

eDP connector

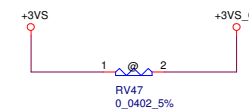


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Touch screen panel power

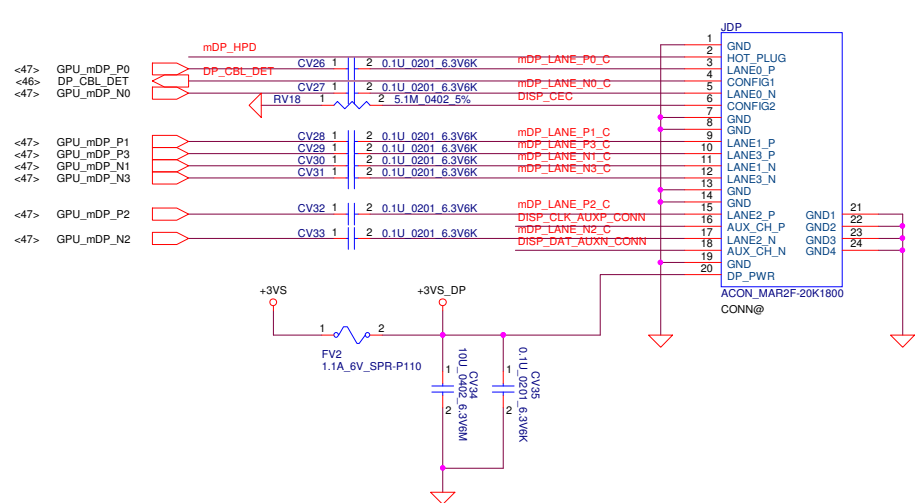


Camera power

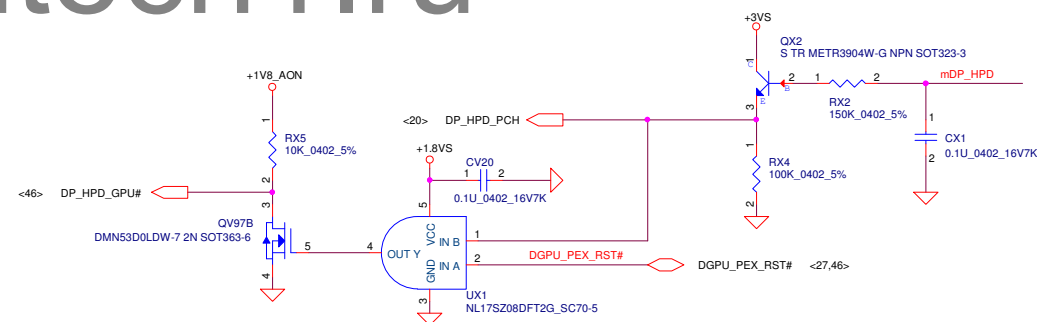


IR camera pindef i ne:
 IR_LED+
 IR_LED+
 IR_LED+/NC
 IR_LED-/DET, connect to PCH GPIO
 IR_LED-
 Diglog_loop, connect to PCH GPIO
 DGND
 D+
 D-
 USB3V3
 MIC_SIG
 MIC_CLK
 DGND

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				Size	Document Number
				LA-D751P	
				Date	Rev
				Tuesday, August 16, 2016	1.0
				Sheet	25 of 82

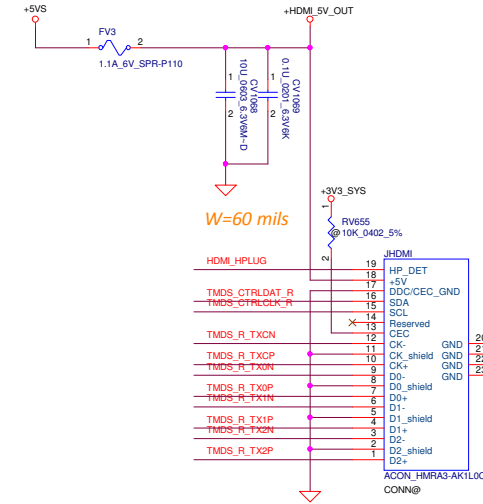
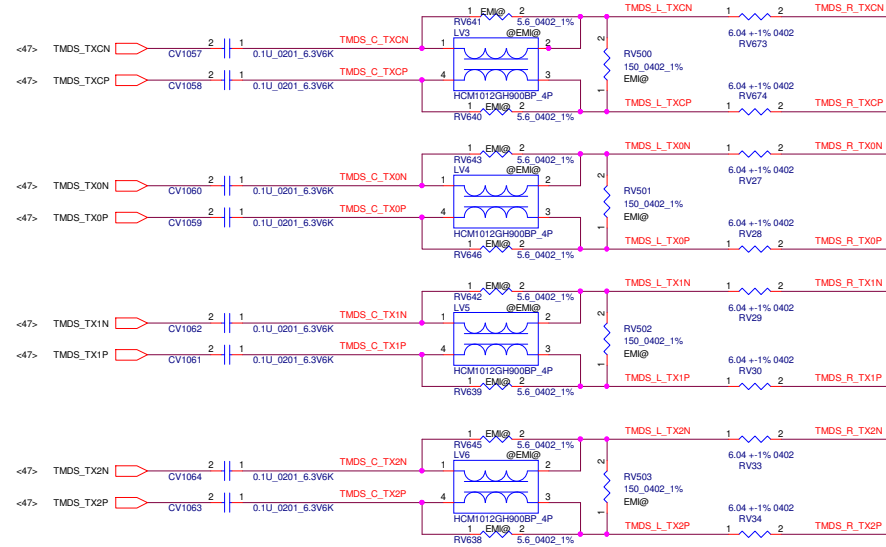


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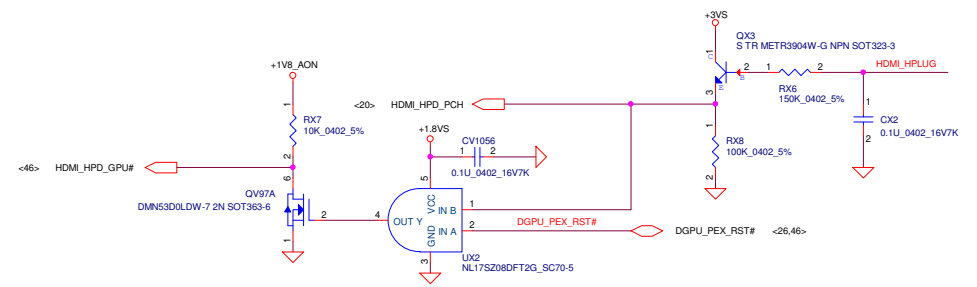
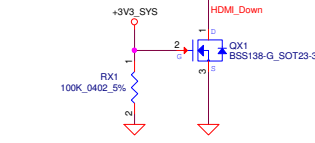
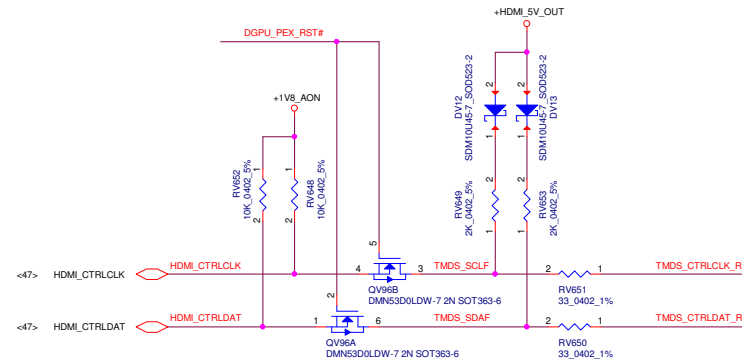


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				Mini DP		
				Size	Document Number	Rev
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Reserve LV3,LV4,LV5,LV6 co-lay with EMI solution @01/12



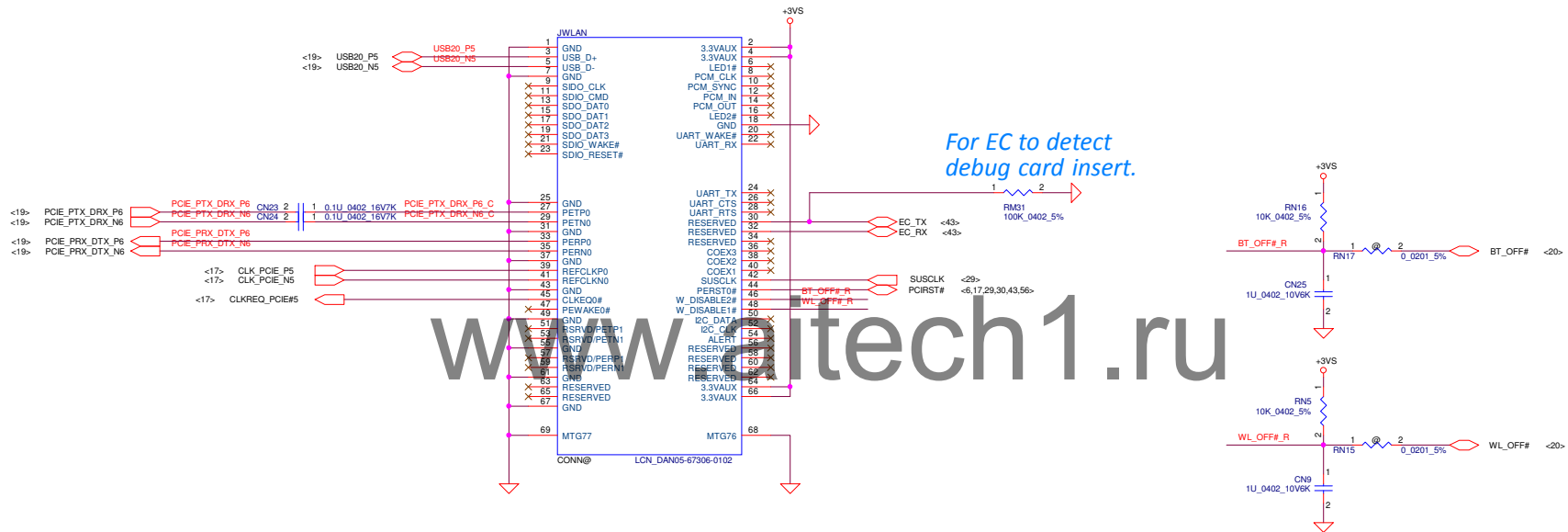
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To GPU

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				Date:	Tuesday, August 16, 2016
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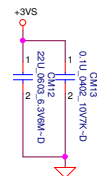
M.2 2230 slot(type E)



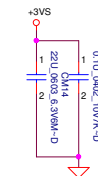
For EC to detect debug card insert.

Prevent backdriver from +3VS_WLAN_NGFF to +3VS

closed to pin 2, 4



closed to pin 64, 66

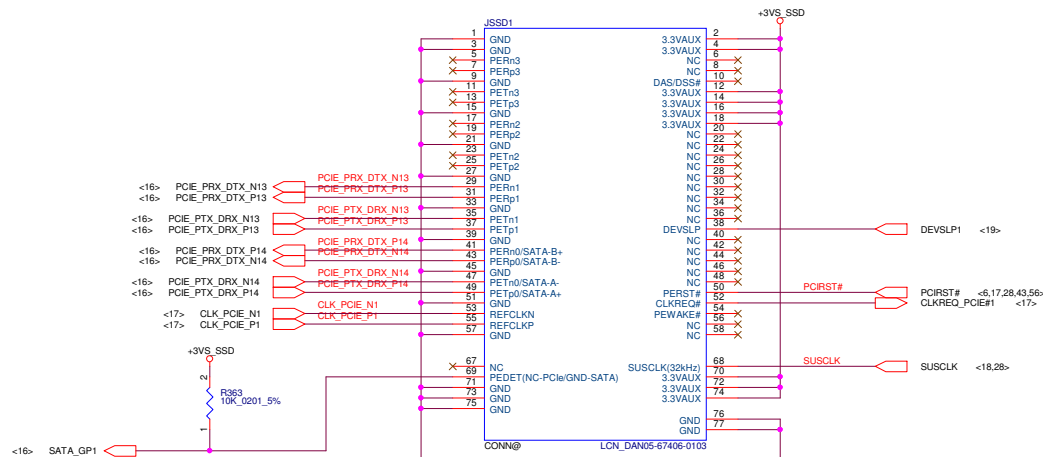


WLAN power control



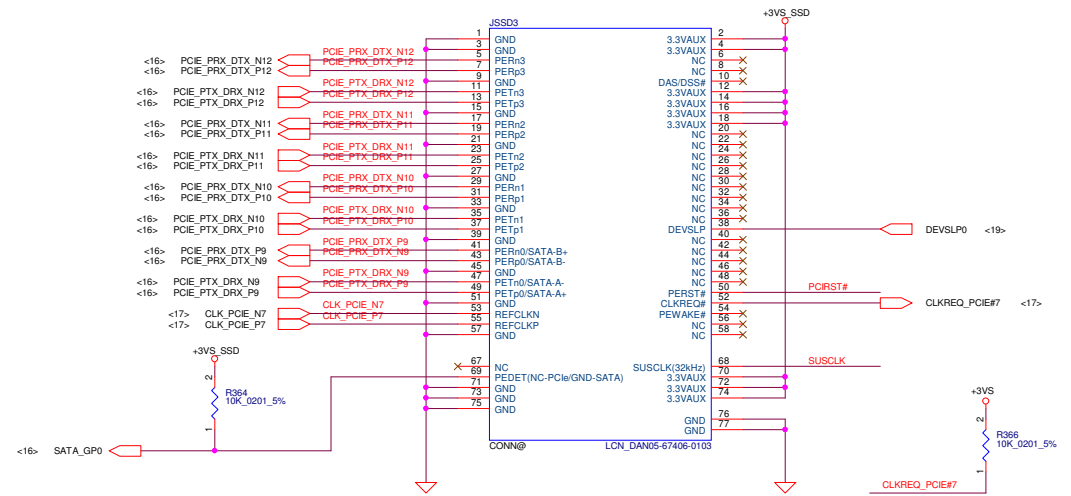
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PCIe/SATA SSD NGFF Slot_1 Key M

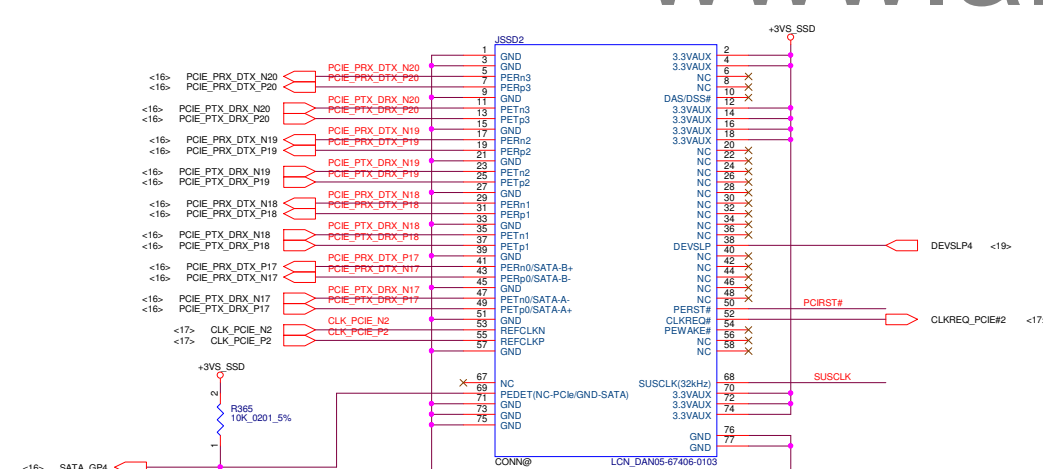


PEDET	Module Type
0	SATA
1	PCIe

PCIe/SATA SSD NGFF Slot_3 Key M

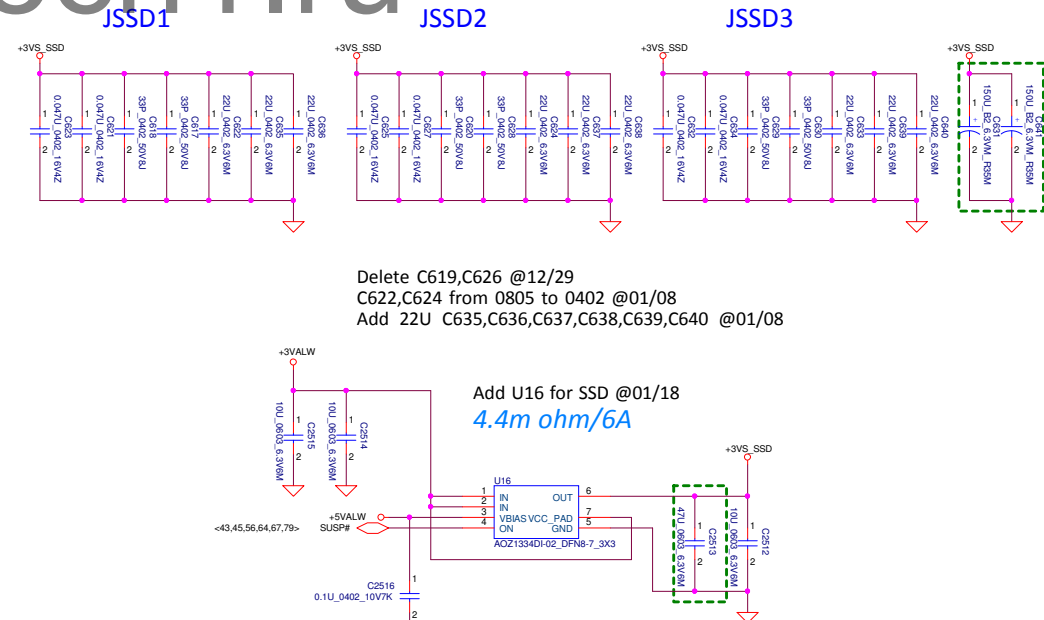


PCIe/SATA SSD NGFF Slot_2 Key M

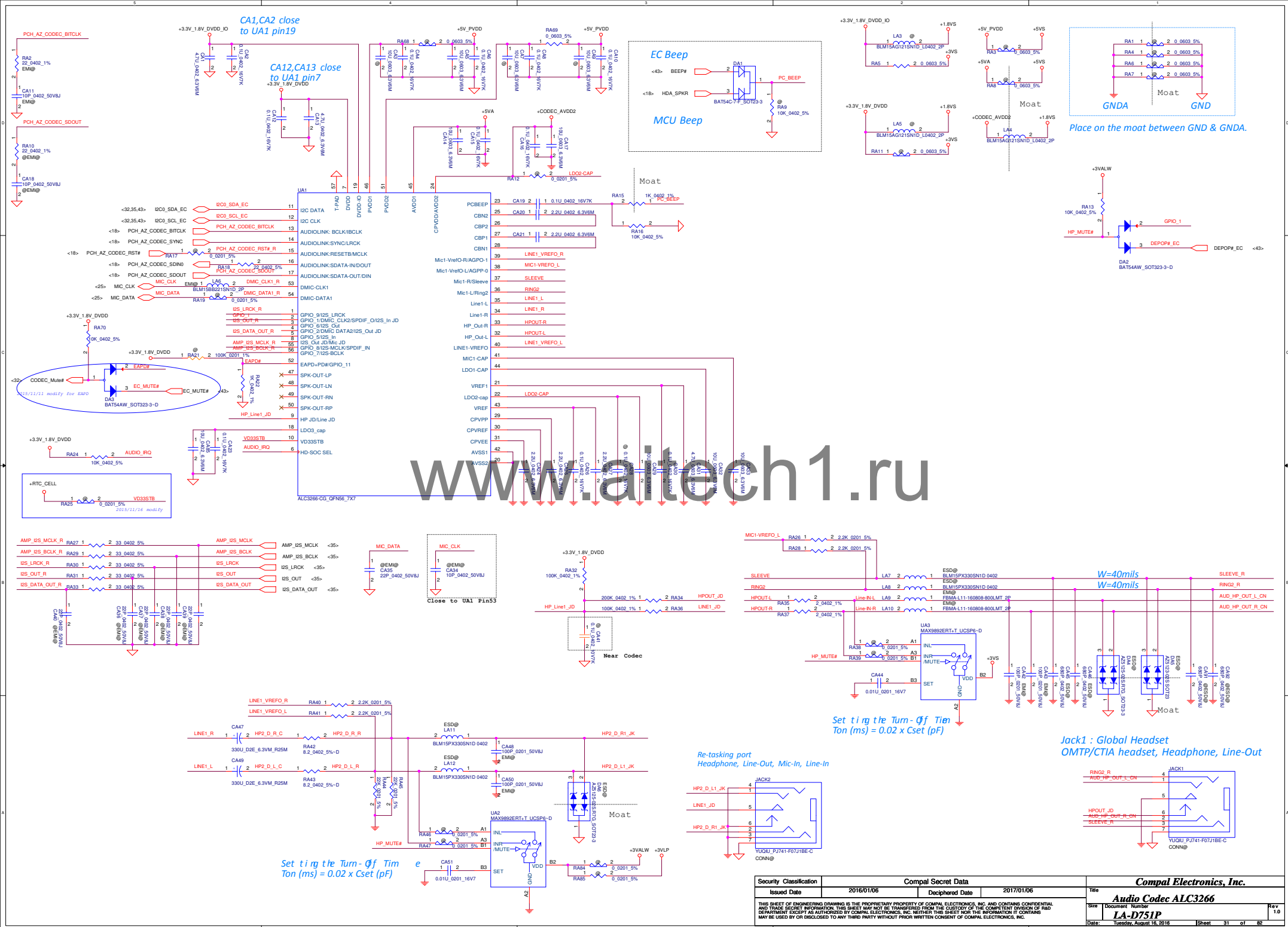


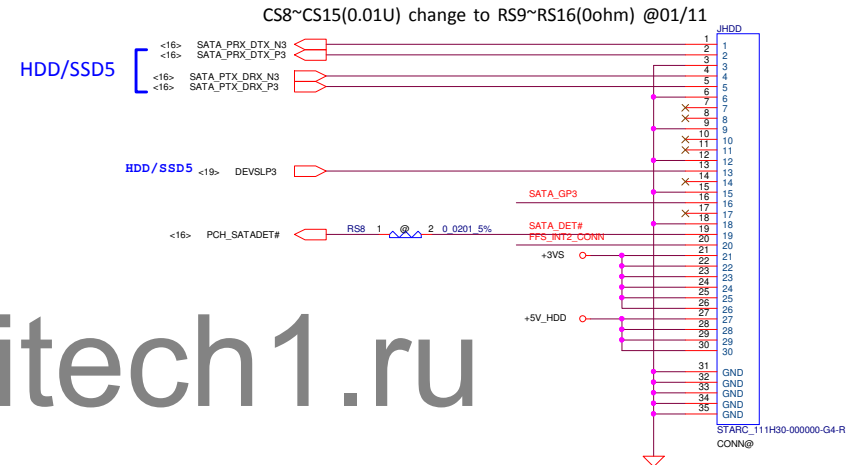
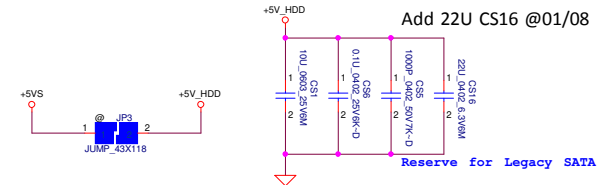
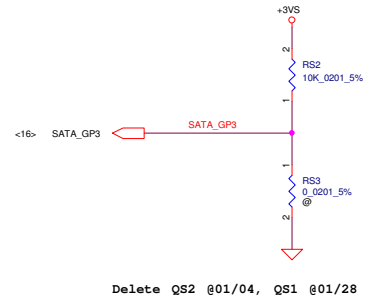
PEDET	Module Type
0	SATA
1	PCIe

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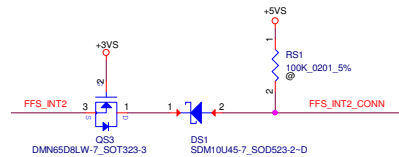
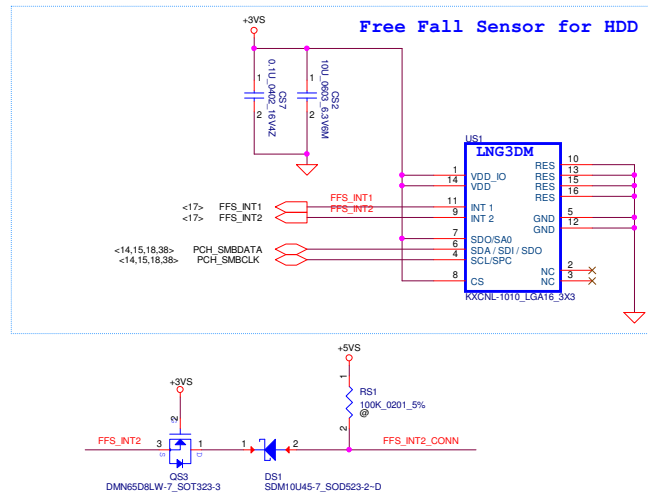


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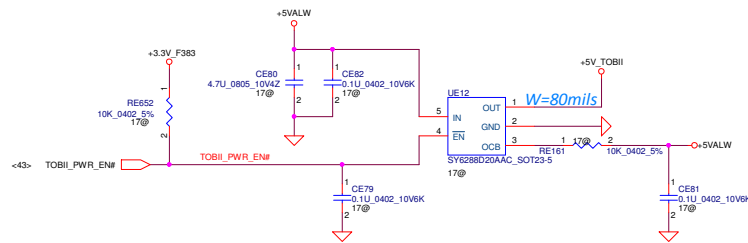


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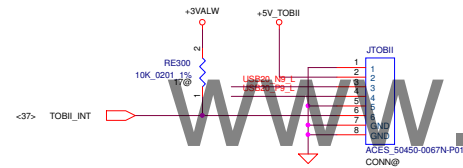
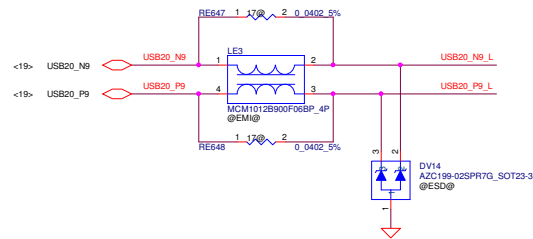


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				Date	Tuesday, August 16, 2016
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				Rev	1.0

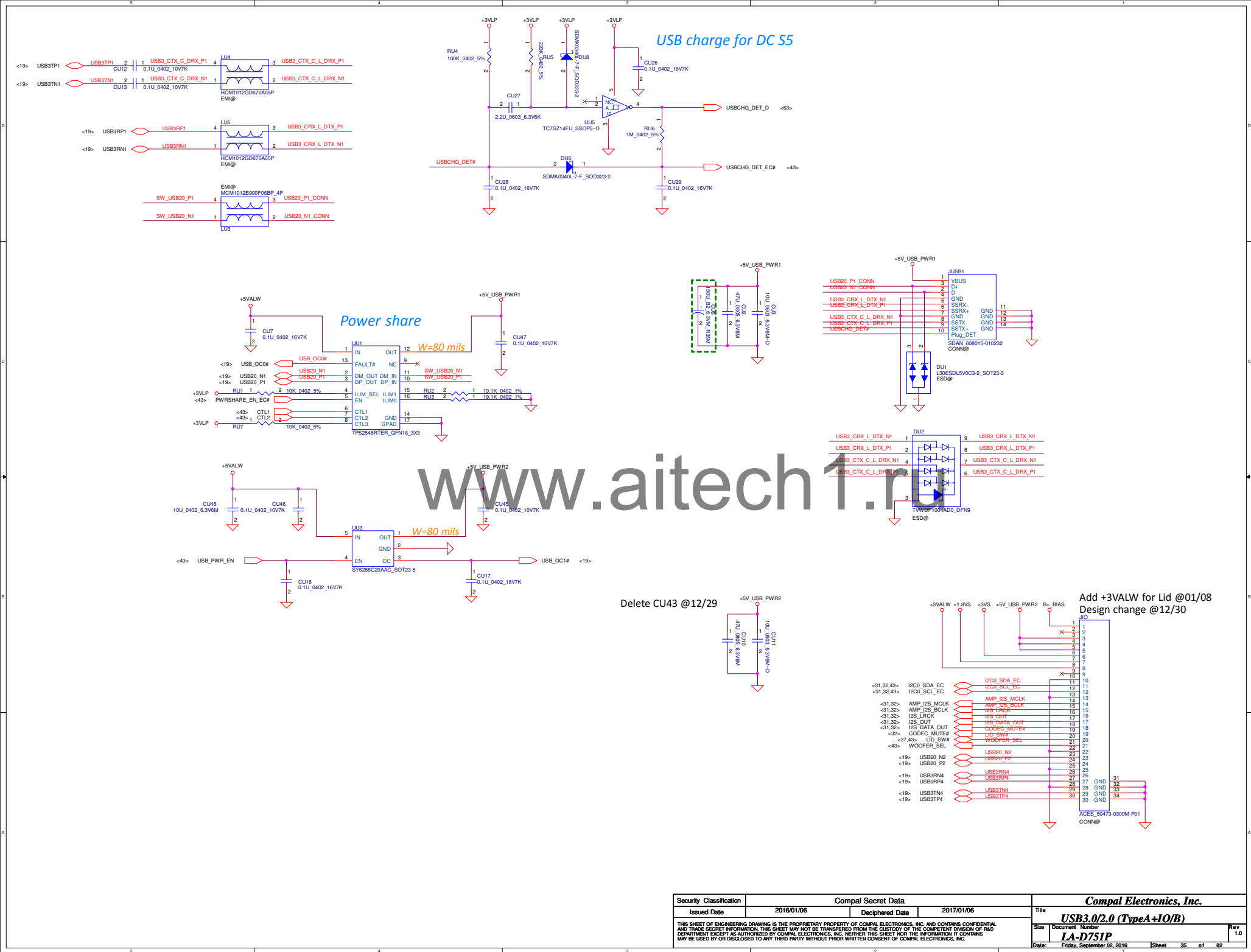
Tobii Conn.

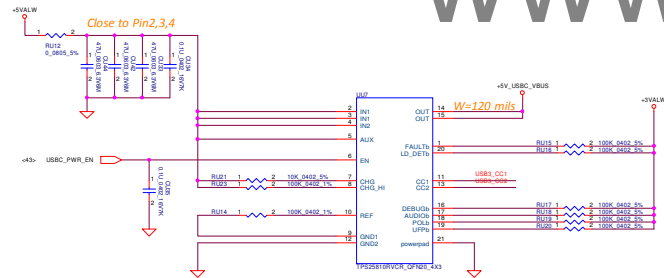
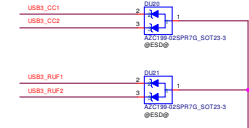
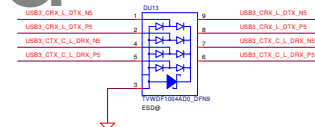
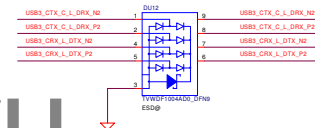
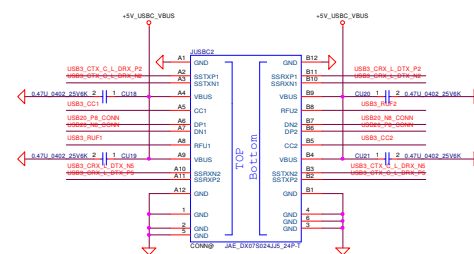
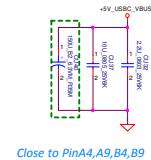
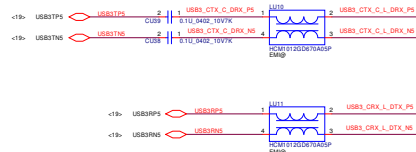
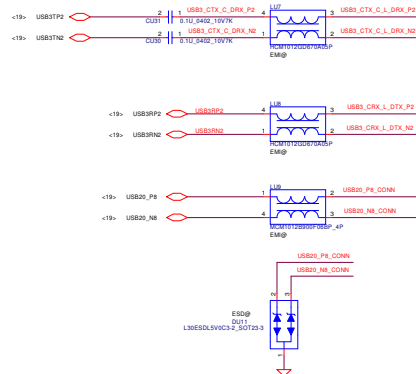


Near JTOBII



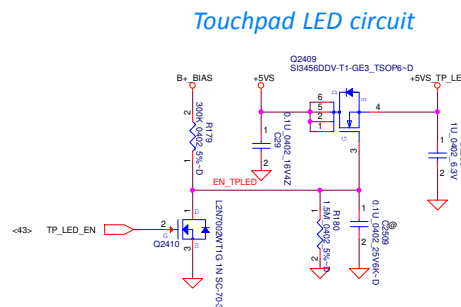
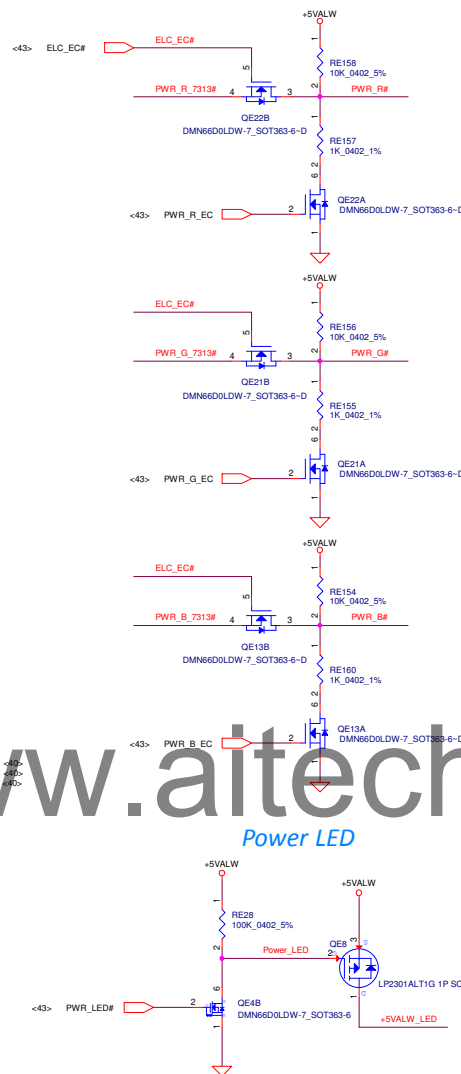
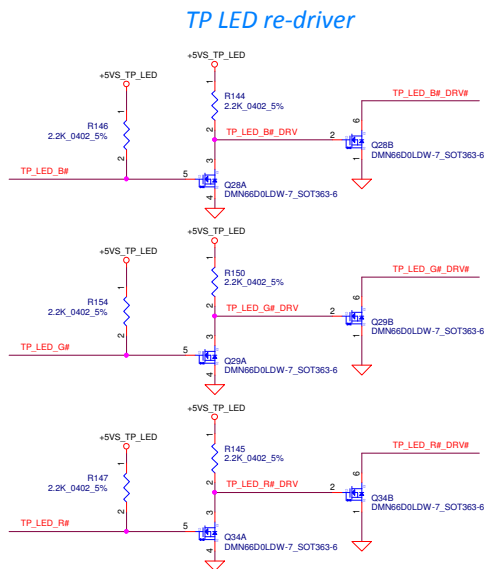
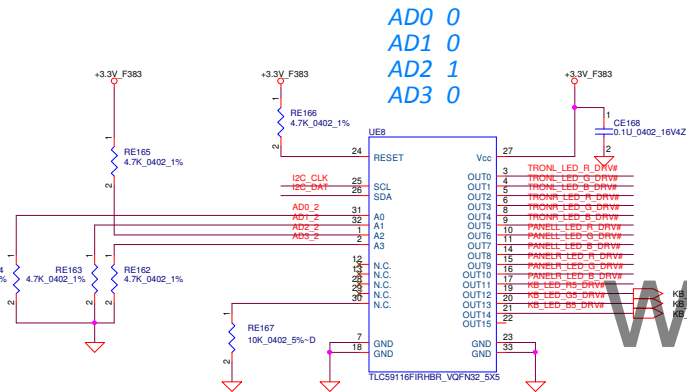
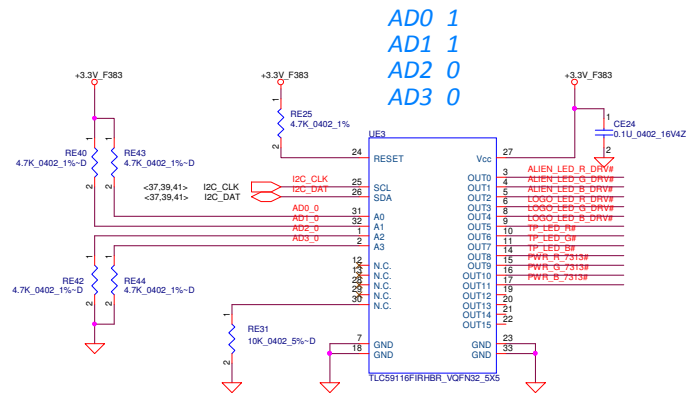
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			Date:	Tuesday, August 16, 2016	
			Sheet	34 of 82	
			Rev	1.0	



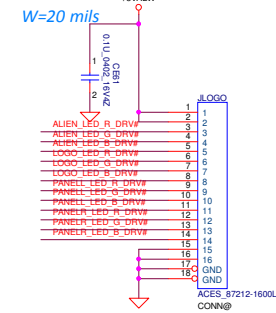


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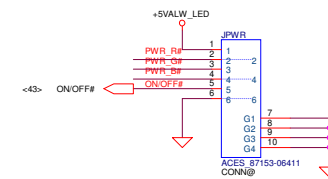
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				USB3.0/2.0 (TypeC)	
				Part No.	
				LA-D751P	
				Date	
				2017/01/06	



To logo board
Change connector from 14pin to 16pin @12/16

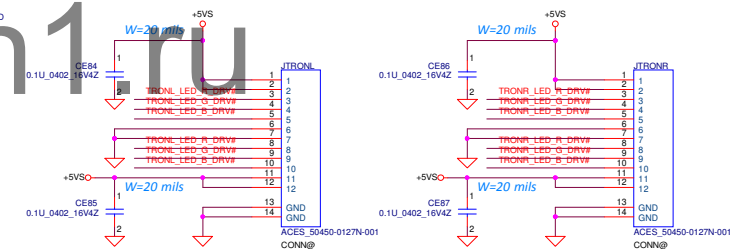


To power board

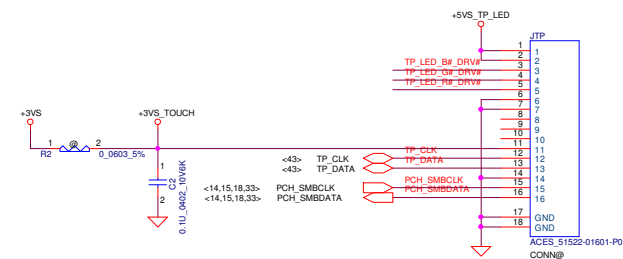


To Tron Light board X2

Change connector from 6pin*4 to 12pin*2 @12/16



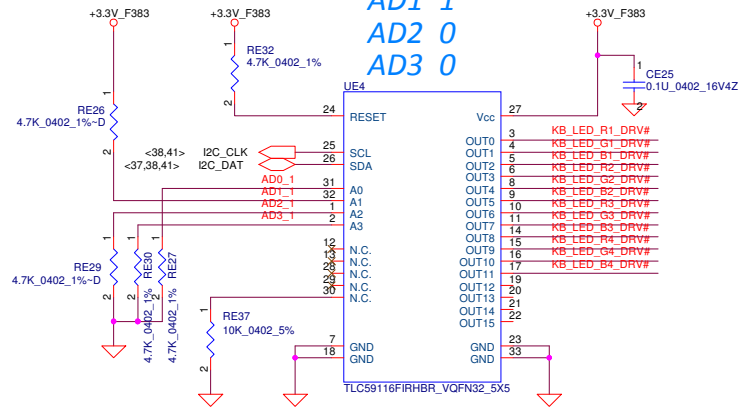
To touchpad module



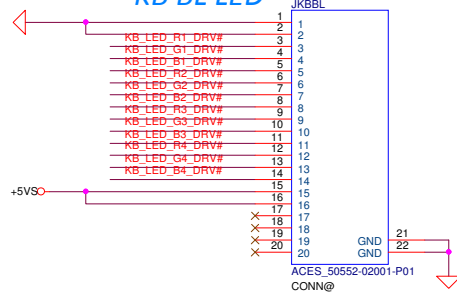
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KB Backlight

AD0 0
AD1 1
AD2 0
AD3 0



KB BL LED

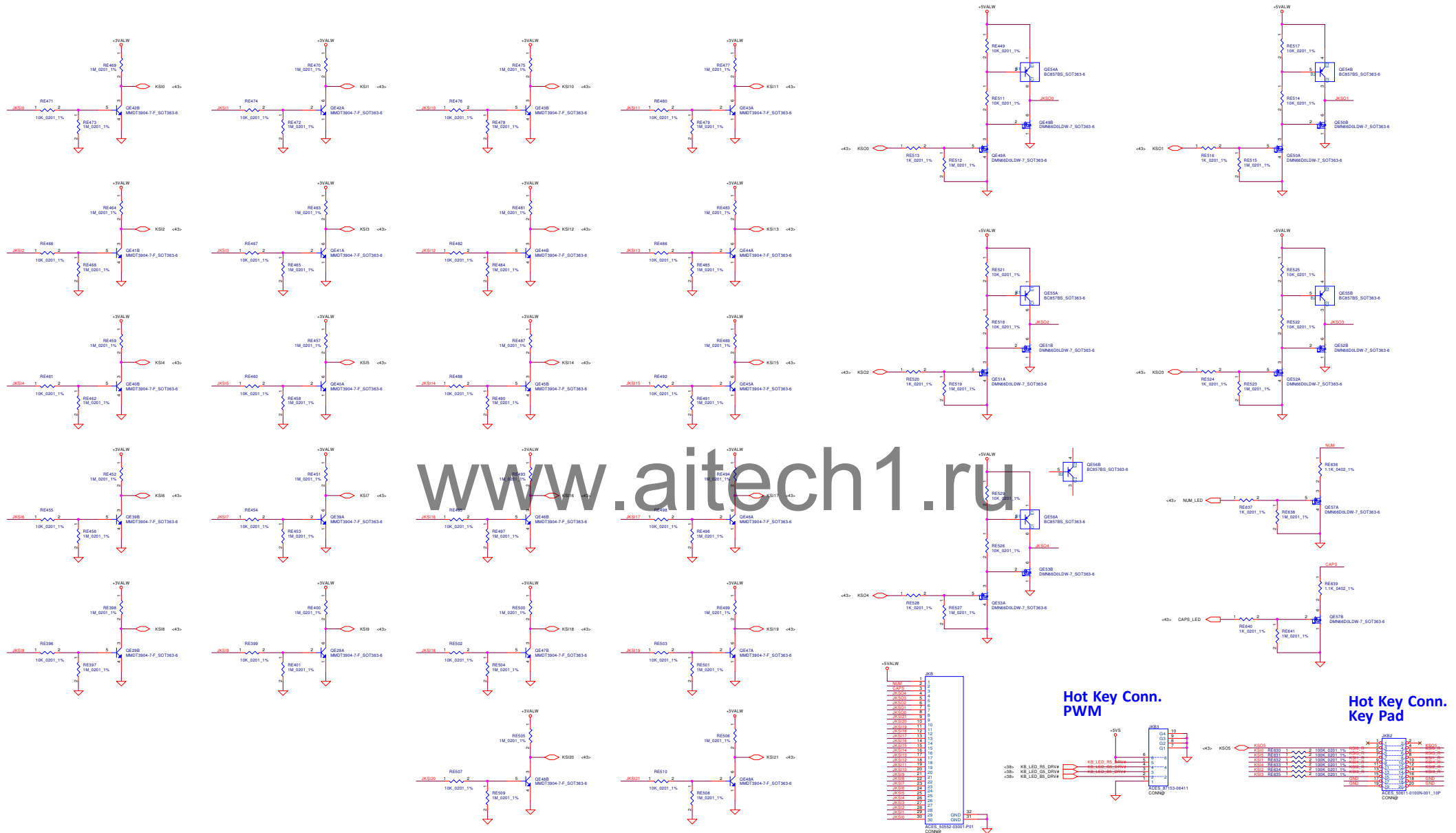


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				Date	Rev
				Tuesday, August 16, 2016	1.0
				Sheet	39 of 82

QE54, QE55, QE56 change to SB000018700

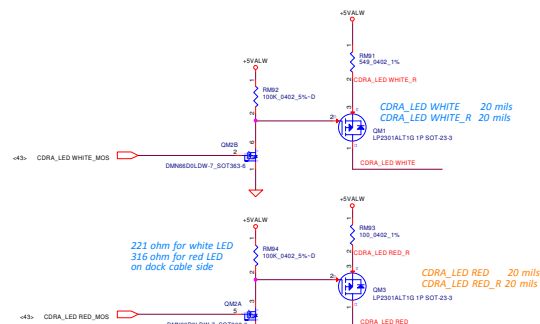
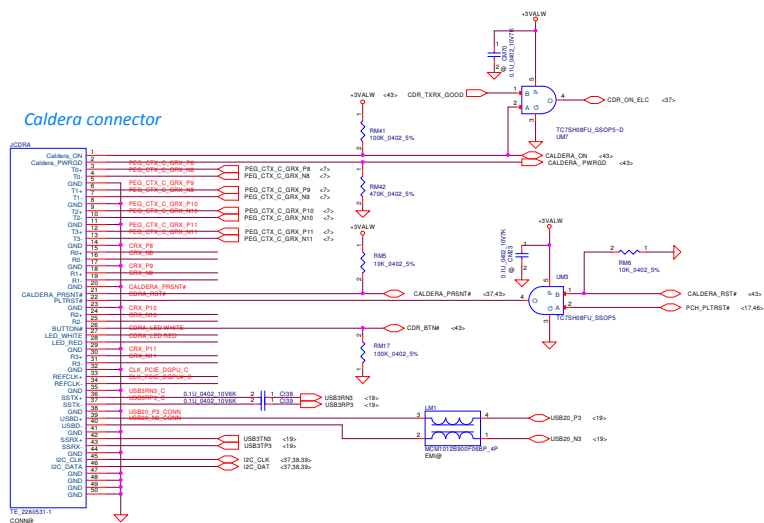
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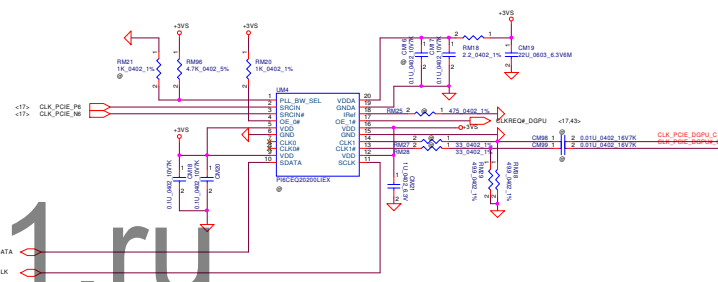
Hot Key Conn. PWM

Hot Key Conn. Key Pad

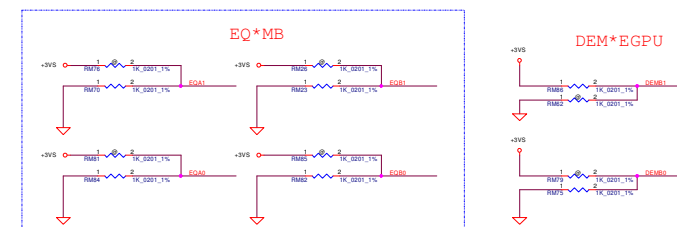
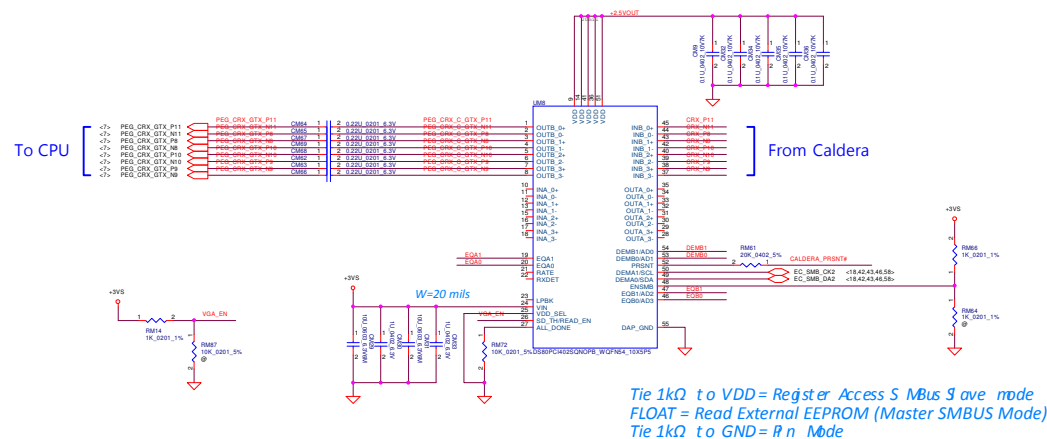
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Issue	1	Issue Date	2017/01/06	Drawn	LA-D75IP



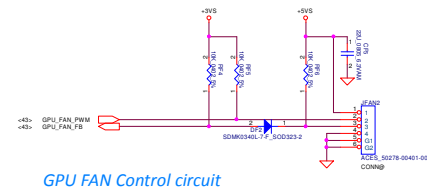
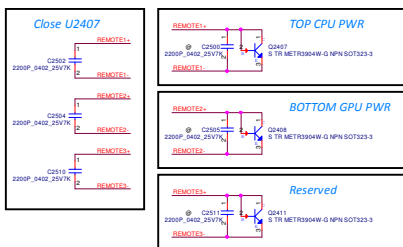
PCIe Clock Buffer	RM25	RM27 / RM28	CM16	CM98 / CM99
Pericom (SA00007J200) X7669431L79	SDQ34475080 (475 +1% 0402)	SD34330A80 (33 +3% 0402)	SE102104K000 (10.1U +10% 0402)	SE076103K80 (0.1U 16V K X7R 0402)
BD (SA00007J200) X7669431L79	SDQ34412080 (412 +1% 0402)	SD00000A080 (27 +1% 0402)	SE000000L010 (1U +10% 0402)	SE076104K80 (1.1U 16V K X7R 0402)



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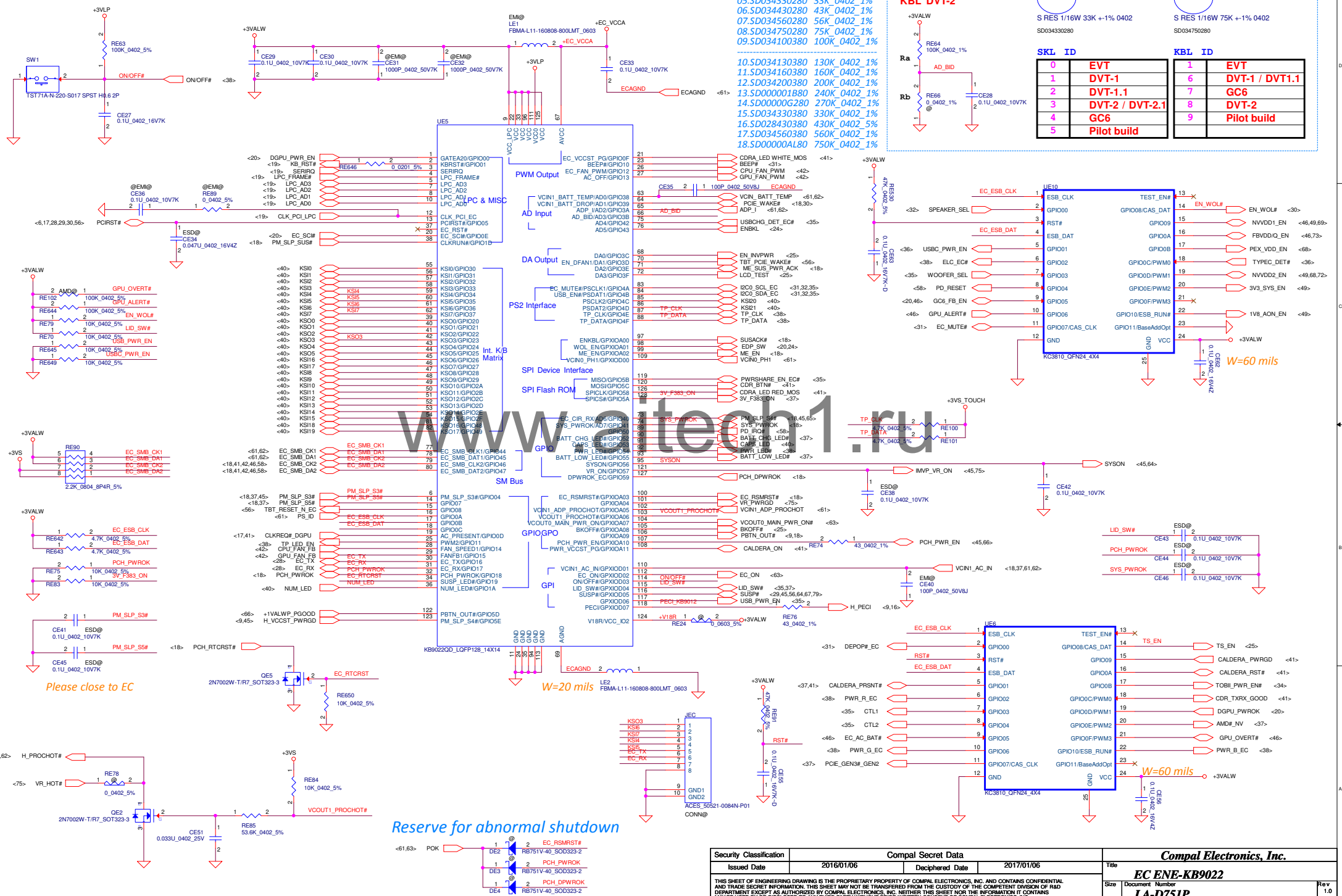
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			LA-0751P	



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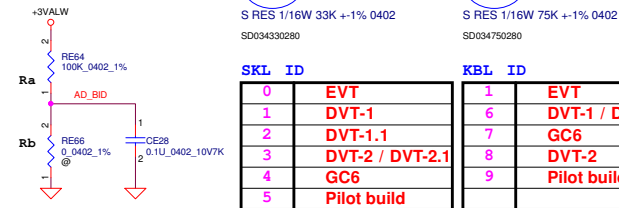
Security Classification	Compul Secret Data		Title	Compul Electronics, Inc. FAN/Thermal
Issued Date	2016/01/06	Deciphered Date		
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Drawn				
Check				

Power ON circuit



Board ID

SKL PVT
KBL DVT-2



0	EVT	1	EVT
1	DVT-1	6	DVT-1 / DVT1.1
2	DVT-1.1	7	GC6
3	DVT-2 / DVT-2.1	8	DVT-2
4	GC6	9	Pilot build
5	Pilot build		

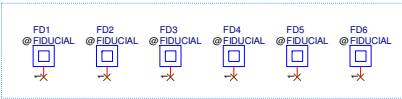
CE62 $W=60$ mils

02_10V7K

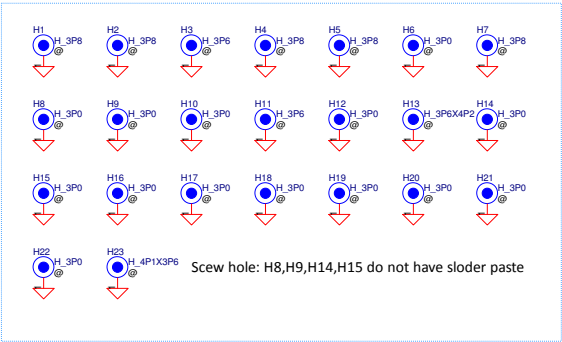
+3VALW

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			LA-D751P	
			Date:	Issued: August 23, 2016
			Rev	1.0

Fiducial Mark

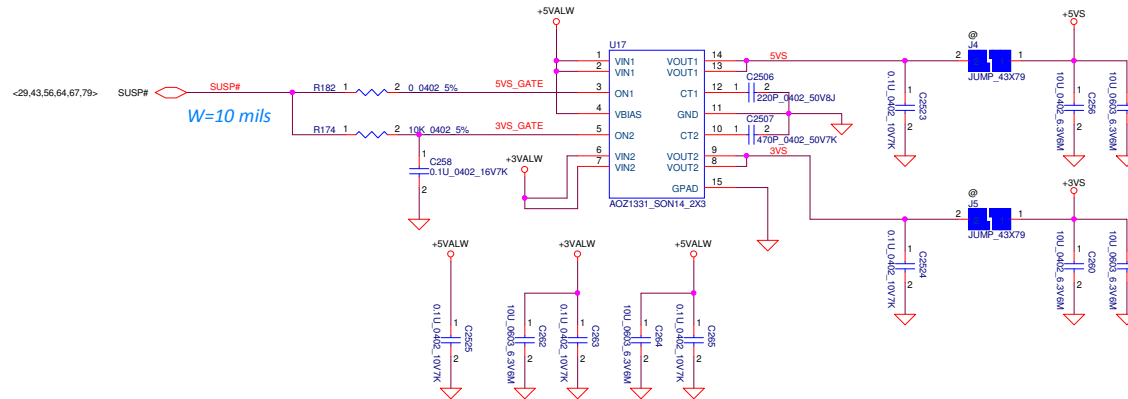


PCB Screw Hole

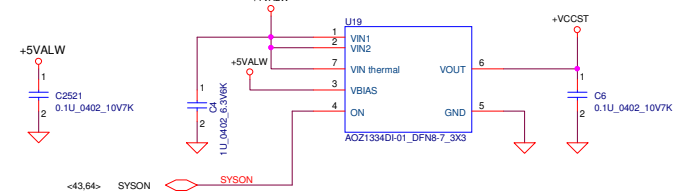


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+5VS and +3VS switch
20mohm/6A per channel



+VCCST switch
4.4mohm/6A
 $TR=12.5\mu s @ V_{in}=1.05V$

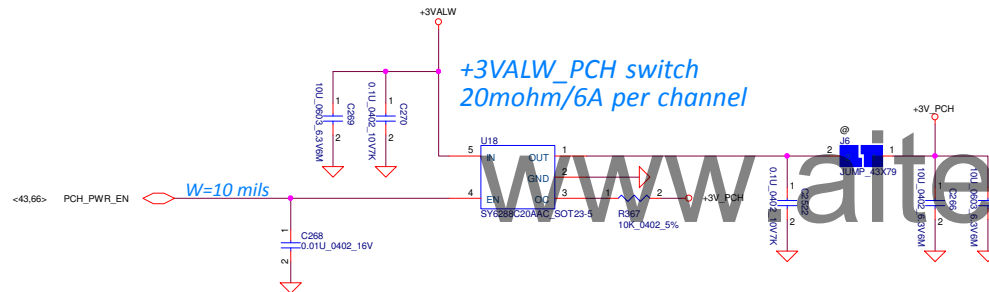


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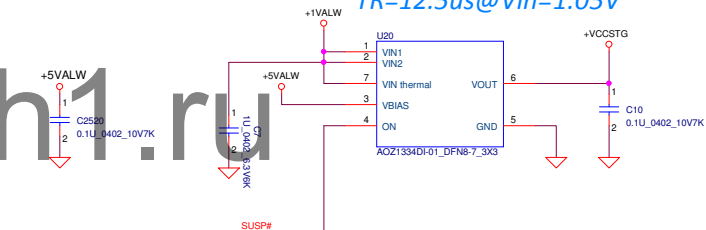
Main source   ACS SA00008A800 (SIC ACZ1334 D-01 DF N8P S NGL LOADS W
2nd source   APEC SA00006V300 (SIC APE8939 GN3 DF N8P LOADS WTCH)
3rd source    EMC SA00008R600 (SIC E M5201V DF NBX3 8P LOADS WTCH)

```

+3VALW_PCH switch
20mohm/6A per channel



+VCCSTG switch
4.4mohm/6A
 $TR=12.5\mu s @ V_{in}=1.05V$



```

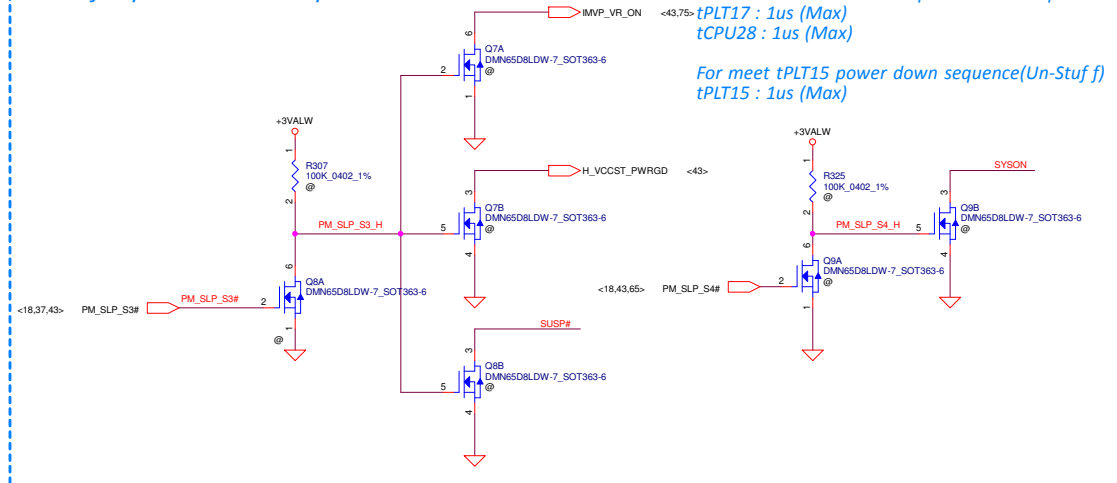
Main source   ACB SA00008A800 (SIC ACZ1334D-01 DFN 8P 9 NGL LOADS W
2nd source   APEC SA00006V300 (SIC APE8939GNB DFN 8P LOADS WTC)
3rd source    EM SA00008R600 (SIC EM5201V DFN 8P 3 8P LOADS WTC)

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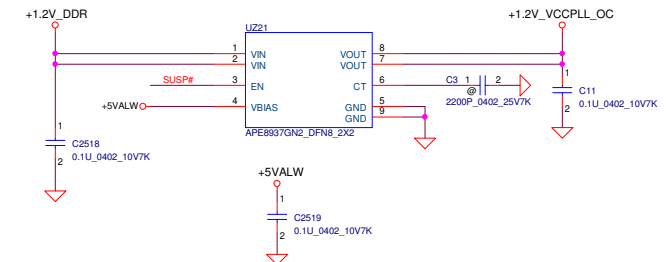
add for power down sequence

For meet tPLT17 & tCPU28 power down sequence.

For meet tPLT15 power down sequence(Un-Stuff)
tPLT15 : 1us (Max)

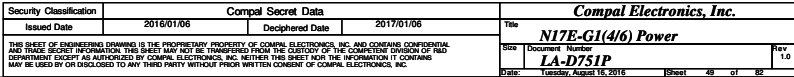


+1.2V_VCCPLL_OC switch
22mohm/4A
TR=520us@Vin=0.8V

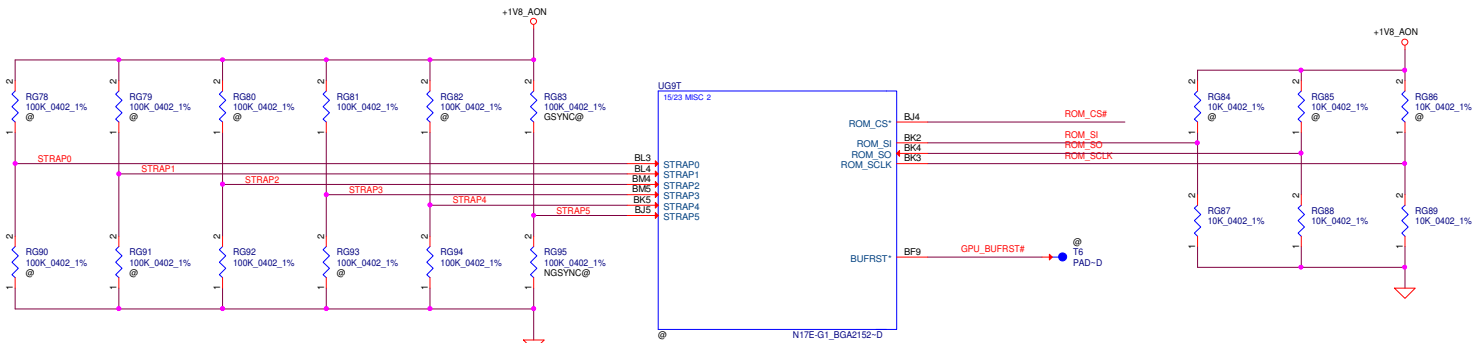


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				Size	Document Number	Rev
				LA-D751P		1.0
Date:	Tuesday, August 16, 2016	Sheet	45	of	80	

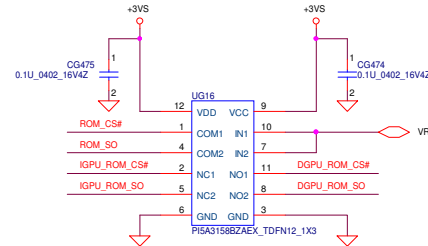
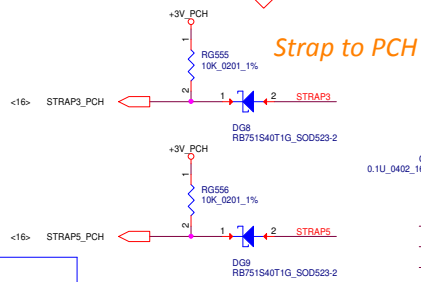




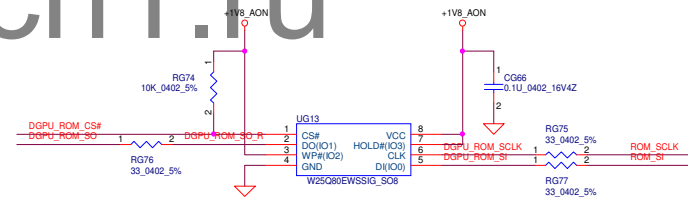
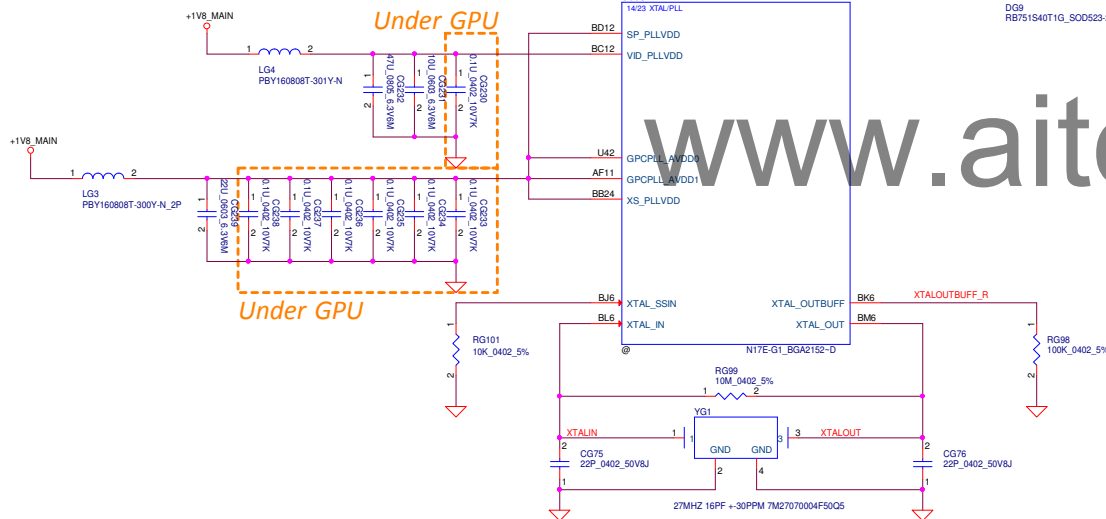
	47uF	22uF	10uF	4.7uF	1uF	0.1uF
VID_PLLVDD	1		1			1
SP_PLLVDD		1				
GPCPLL_AVDD						6



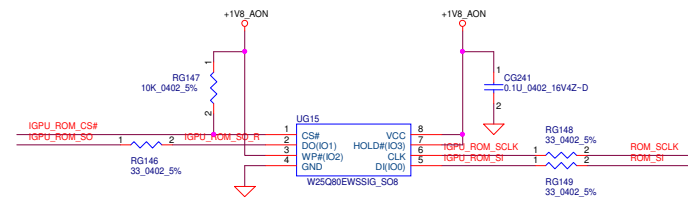
GDDR5 VRAM	Strap0	Strap1	Strap2	Strap3	Strap4	Strap5	RAMCFG
SAMSUNG K4G80325FB-HC25	L	L	L	H	L		0
SAMSUNG K4G4325FE-HC28							
MICRON MT51J256M32HF-80:A	H	L	L	H	L		1
HYNIX H5GC4H24AJR-R0C	L	H	L	H	L		2



Function	VROM_SEL
COM = NC	L
COM = NO	H

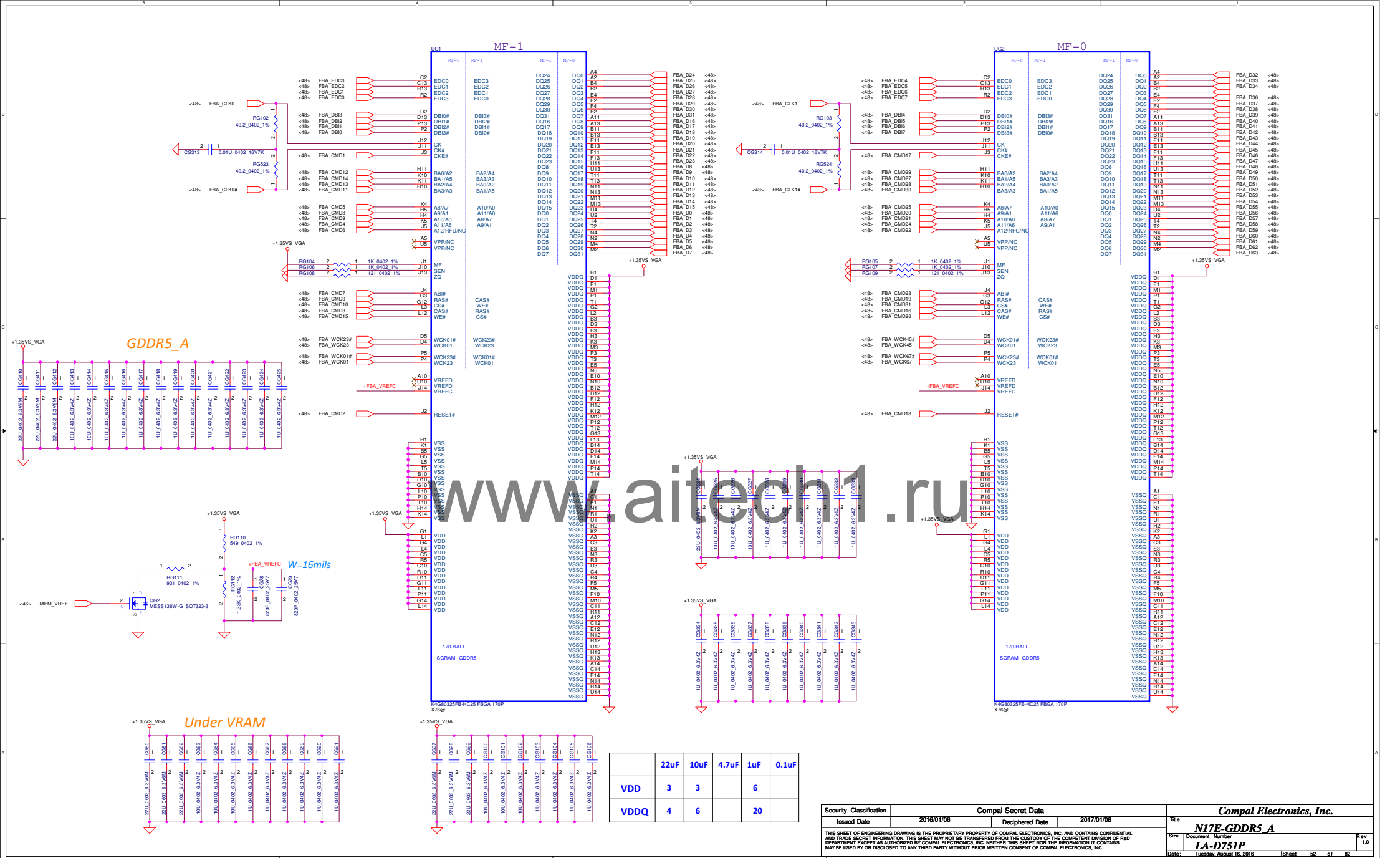


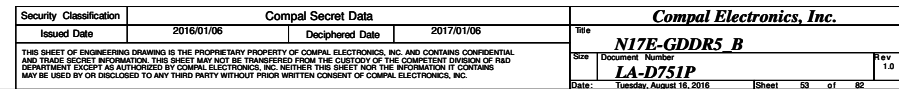
DGPU VBIOS ROM

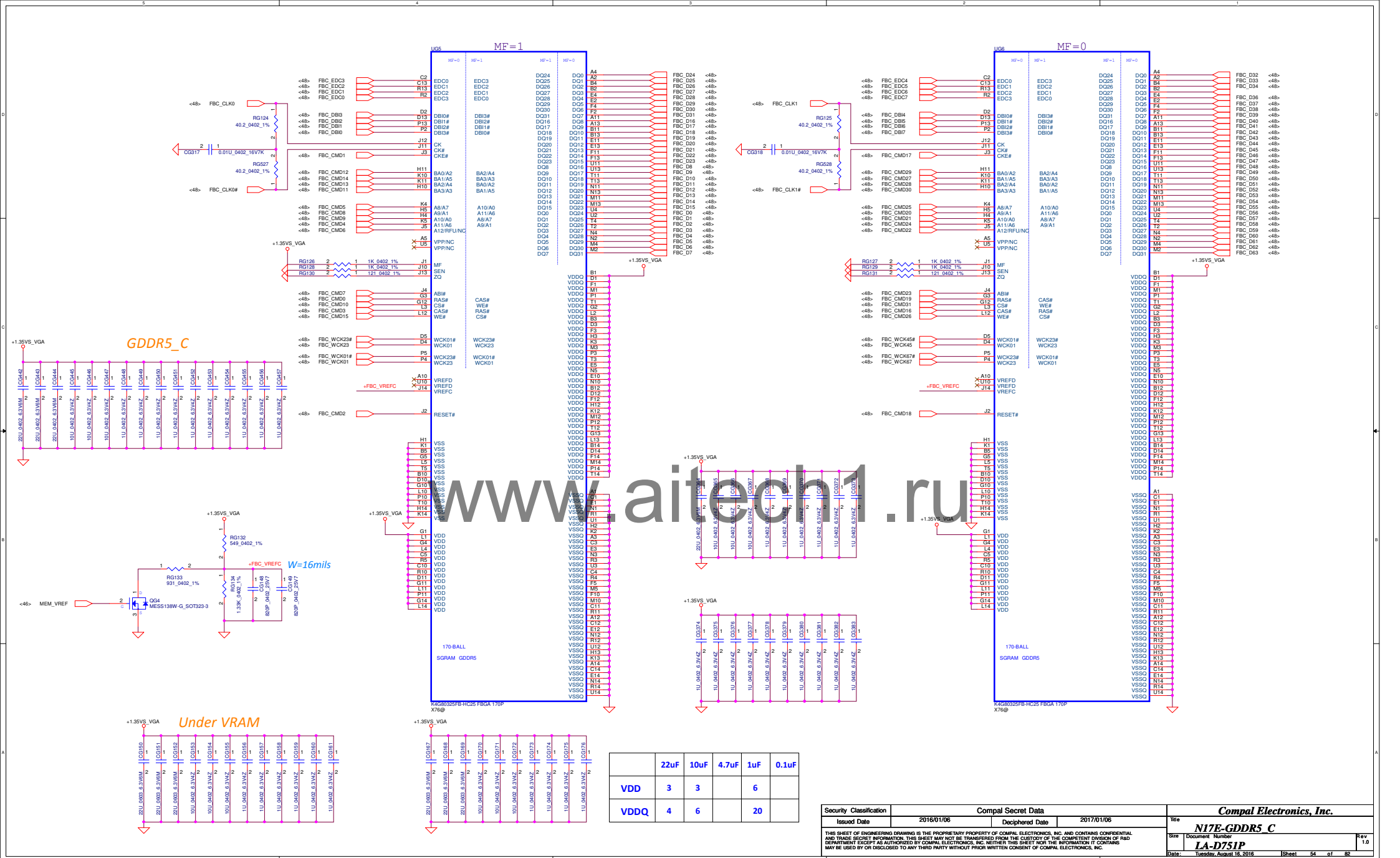


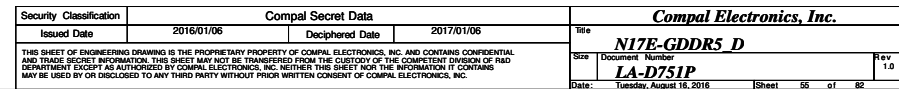
Opt i ms VB OS ROM

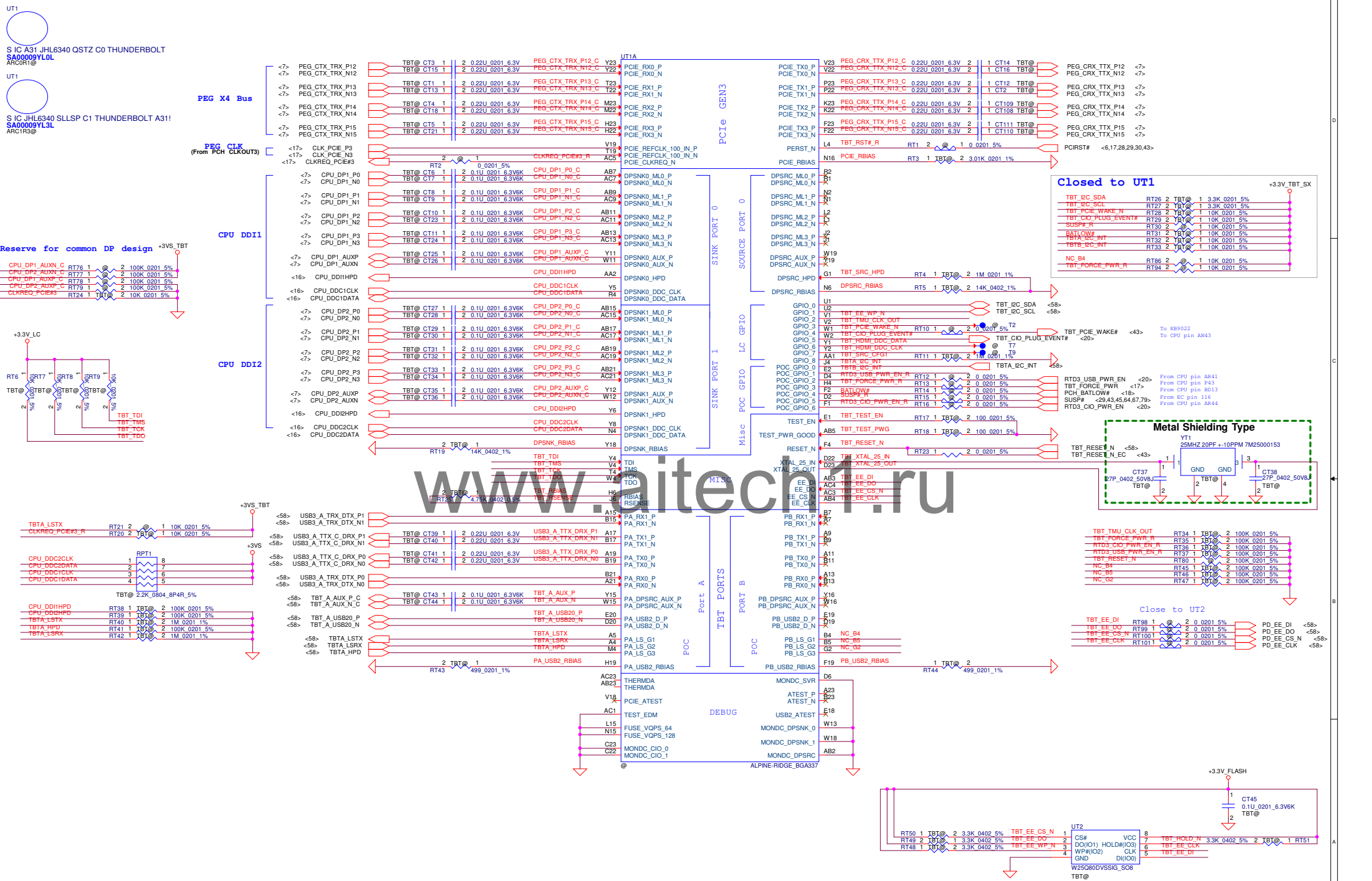
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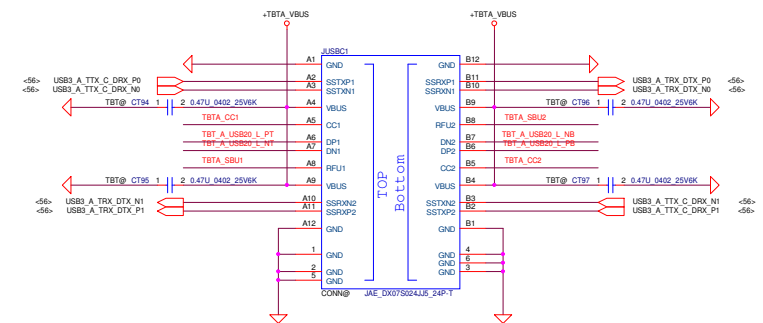
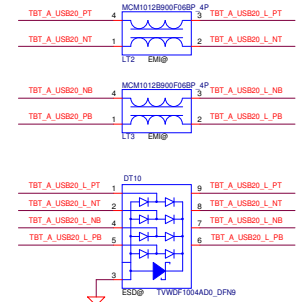
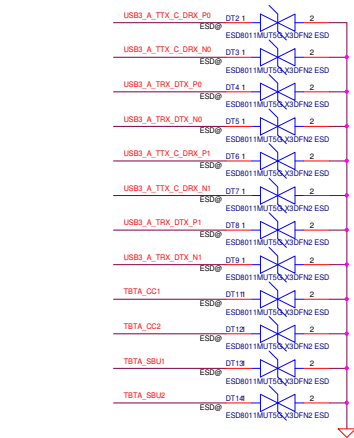
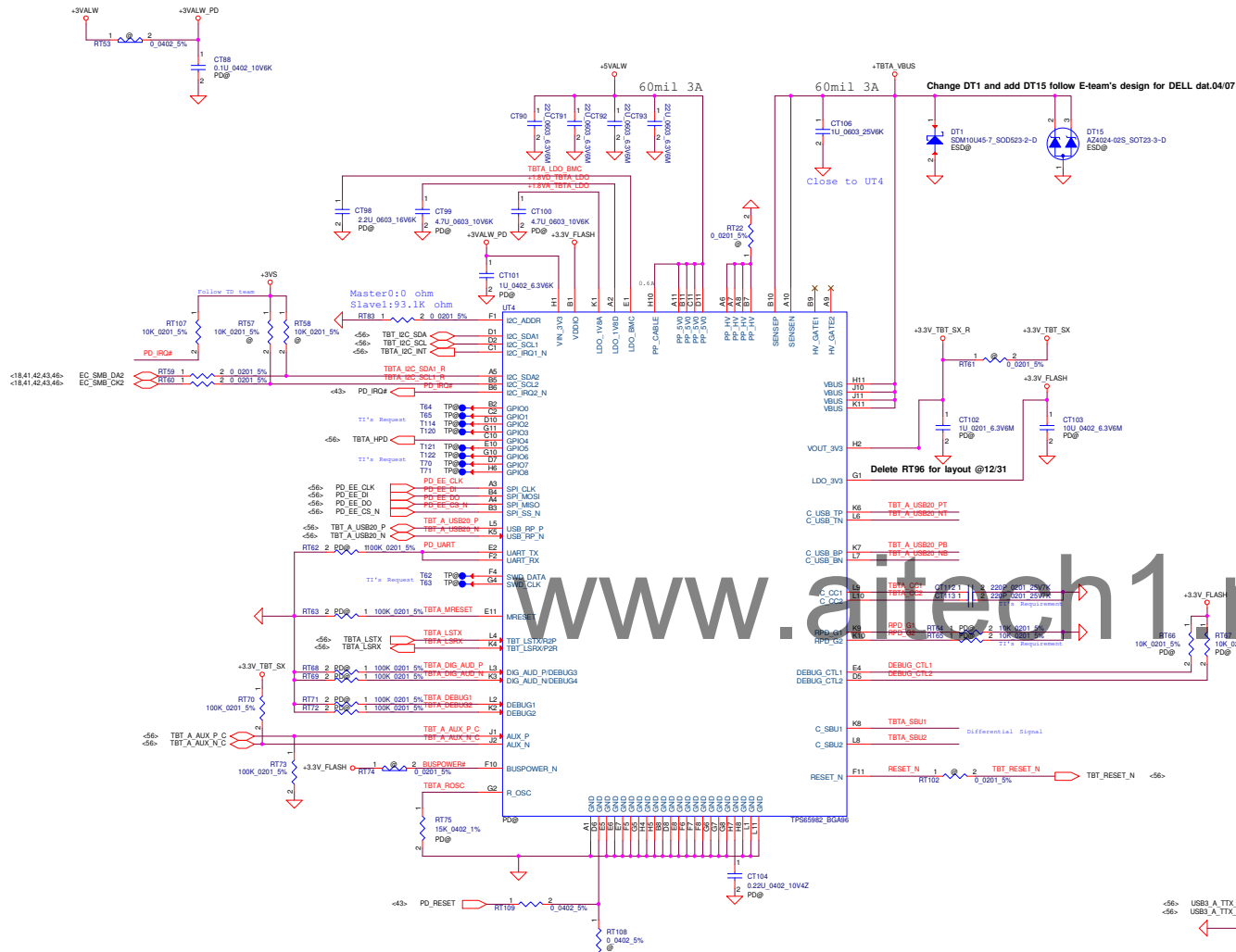


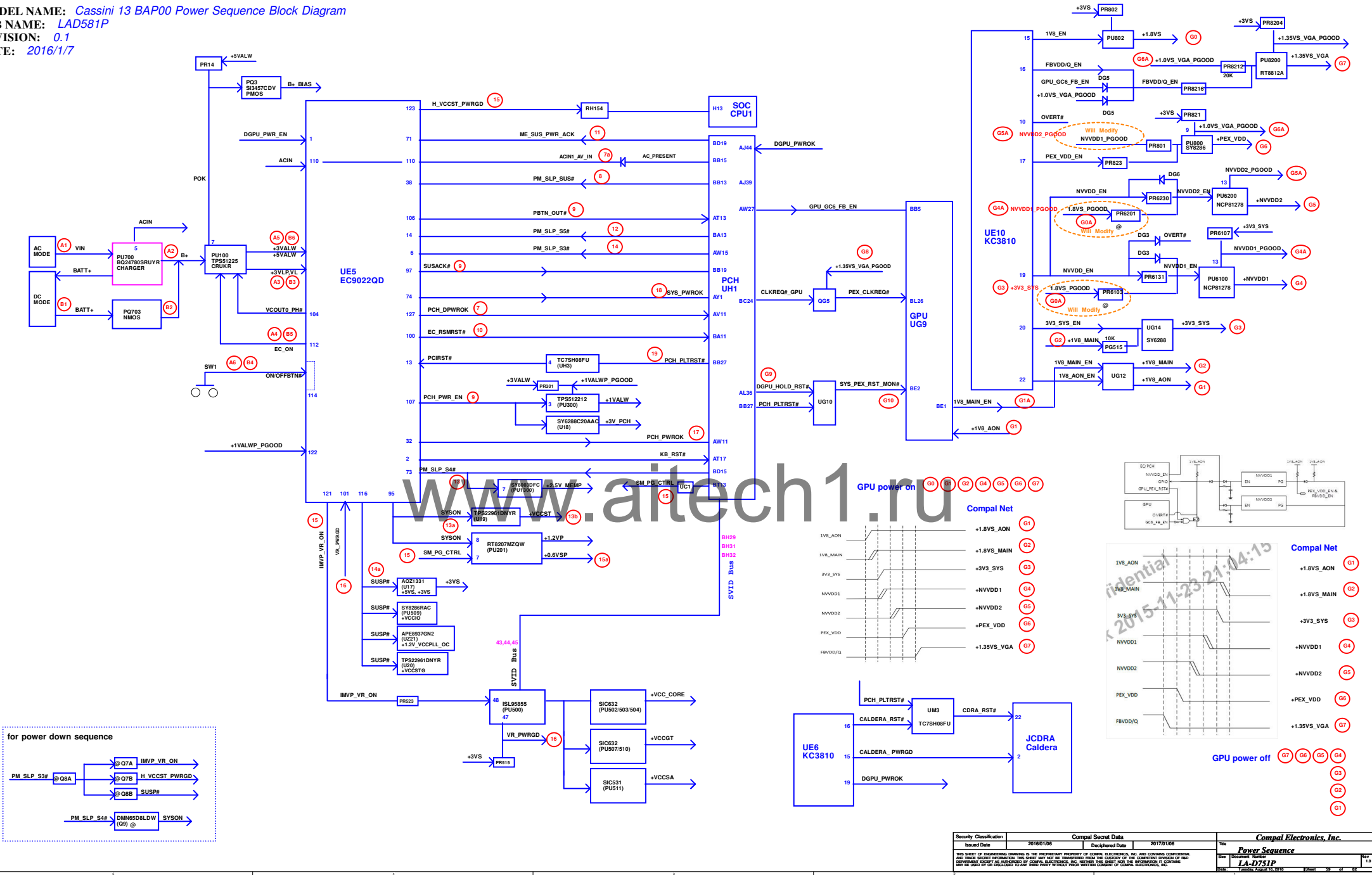
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Delete RT52 for layout @12/31



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					LA-D751P	1.0
Date:				Tuesday, August 16, 2016	Sheet	57 of 82



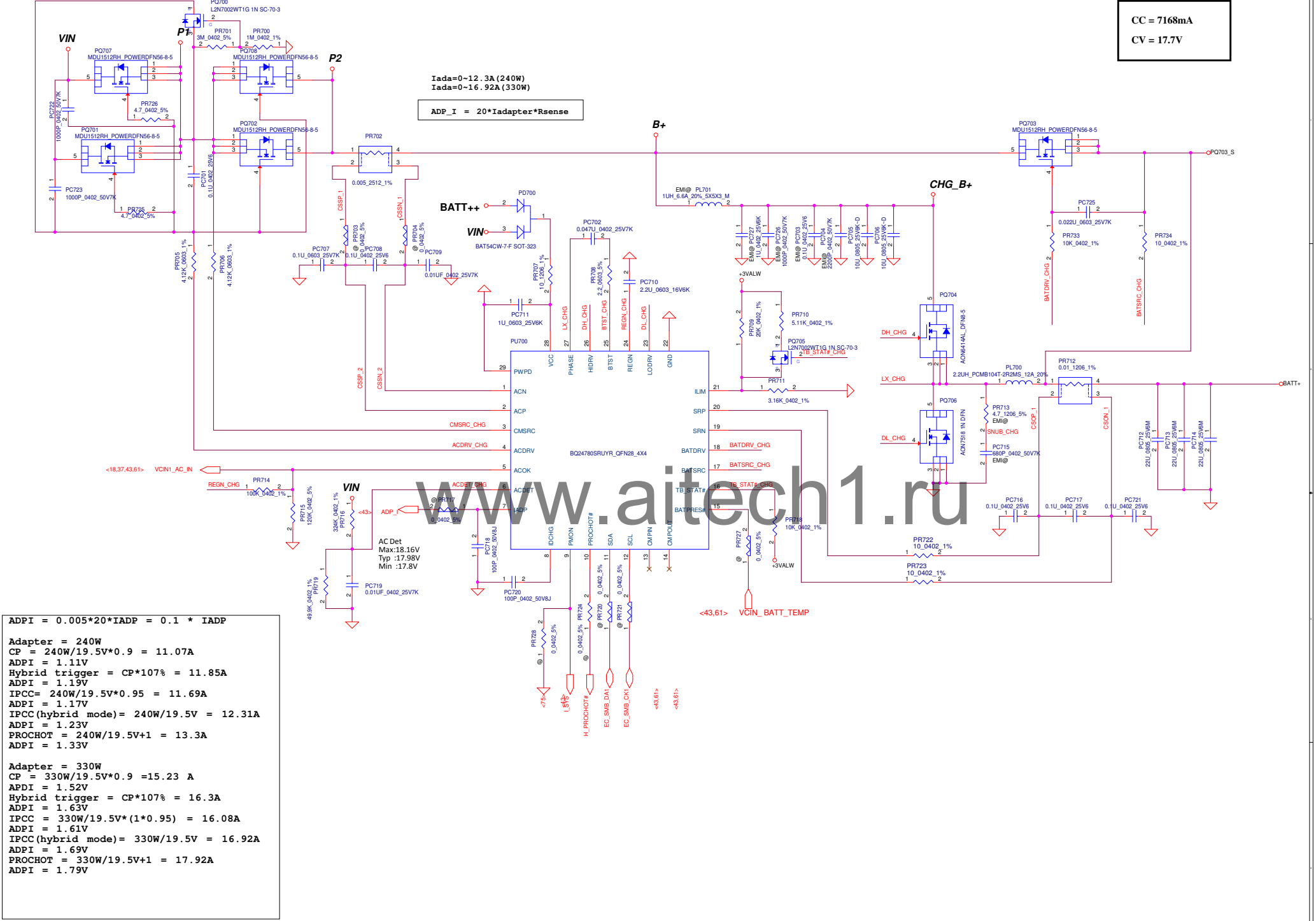




Iada=0~12.3A (240W)
Iada=0~16.92A (330W)

ADP_I = 20*Iadapter*Rsense

CC = 7168mA
CV = 17.7V

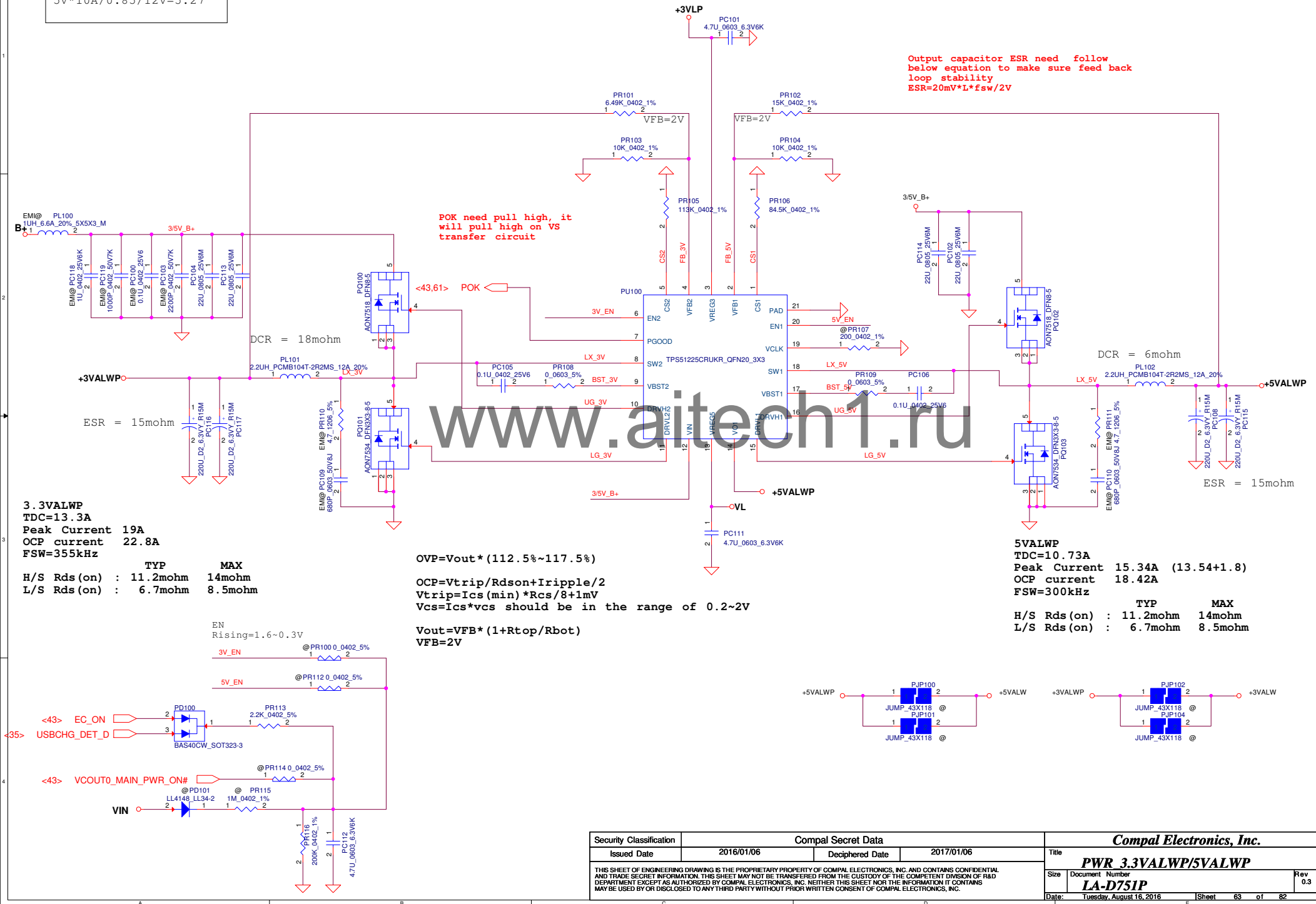


ADPI = 0.005*20*IADP = 0.1 * IADP

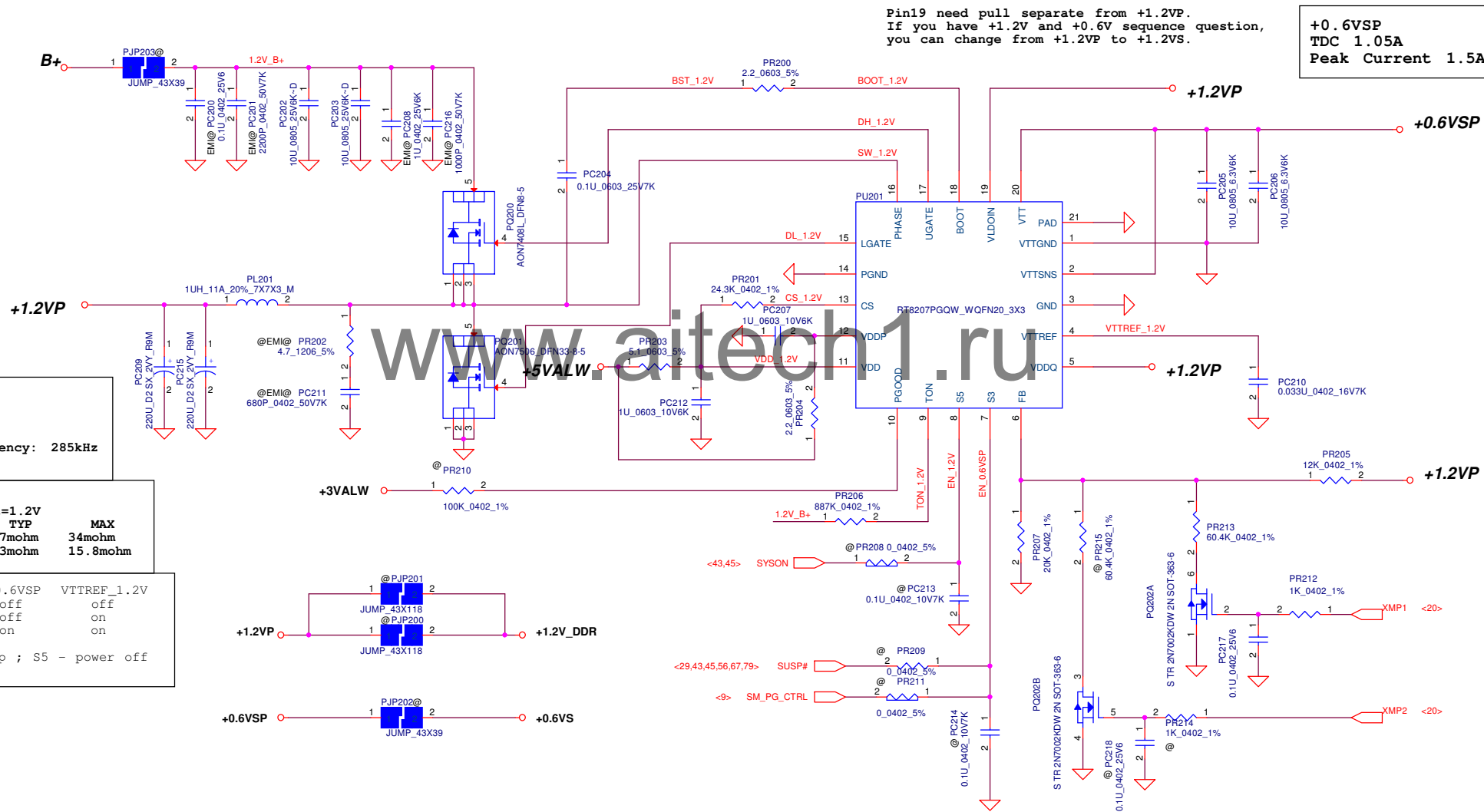
Adapter = 240W
CP = 240W/19.5V*0.9 = 11.07A
ADPI = 1.11V
Hybrid trigger = CP*107% = 11.85A
ADPI = 1.19V
IPCC = 240W/19.5V*0.95 = 11.69A
ADPI = 1.17V
IPCC(hybrid mode) = 240W/19.5V = 12.31A
ADPI = 1.23V
PROCHOT = 240W/19.5V+1 = 13.3A
ADPI = 1.33V

Adapter = 330W
CP = 330W/19.5V*0.9 = 15.23 A
ADPI = 1.52V
Hybrid trigger = CP*107% = 16.3A
ADPI = 1.63V
IPCC = 330W/19.5V*(1+0.95) = 16.08A
ADPI = 1.61V
IPCC(hybrid mode) = 330W/19.5V = 16.92A
ADPI = 1.69V
PROCHOT = 330W/19.5V+1 = 17.92A
ADPI = 1.79V

Input Current: 7.5A
 $3.3V \cdot 10A / 0.85 / 12V = 2.23$
 $5V \cdot 10A / 0.85 / 12V = 5.27$



Input Current: 1A
 $1.2V \cdot 8.88A / 0.85 / 12V = 1$



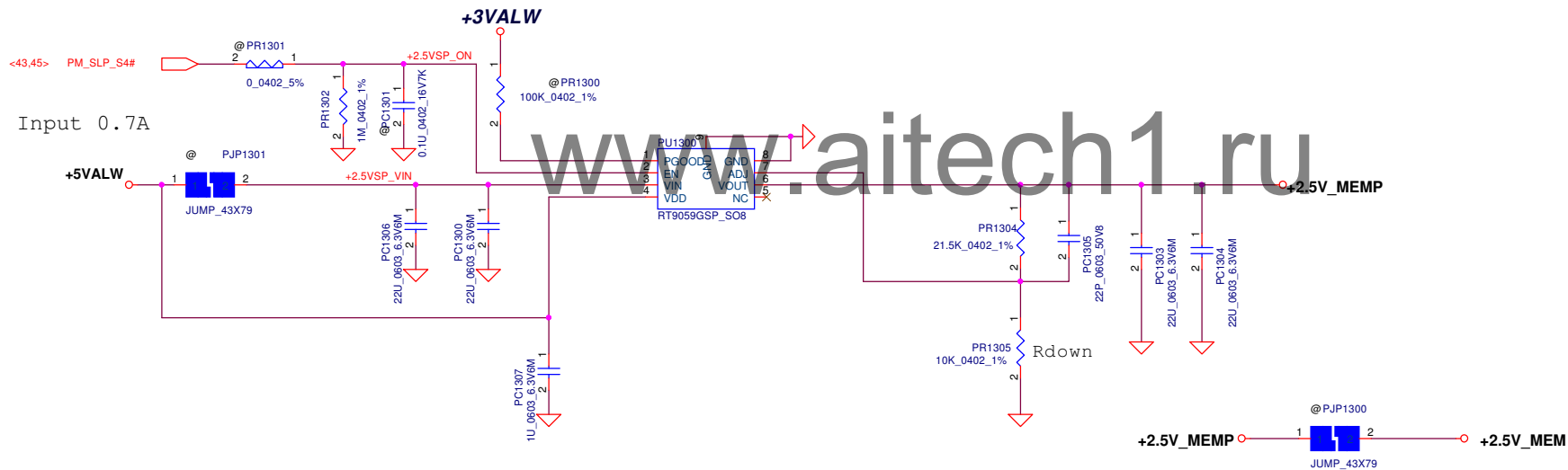
+1.2VP
TDC=9A
Ipeak=12.86A
OCP=15.43A
Switching Frequency: 285kHz

OVP: 110%~120%	
VFB=0.75V, Vout=1.2V	
	TYP MAX
H/S Rds (on) :	27mohm 34mohm
L/S Rds (on) :	13mohm 15.8mohm

Mode	Level	+0.6VSP	VTTREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

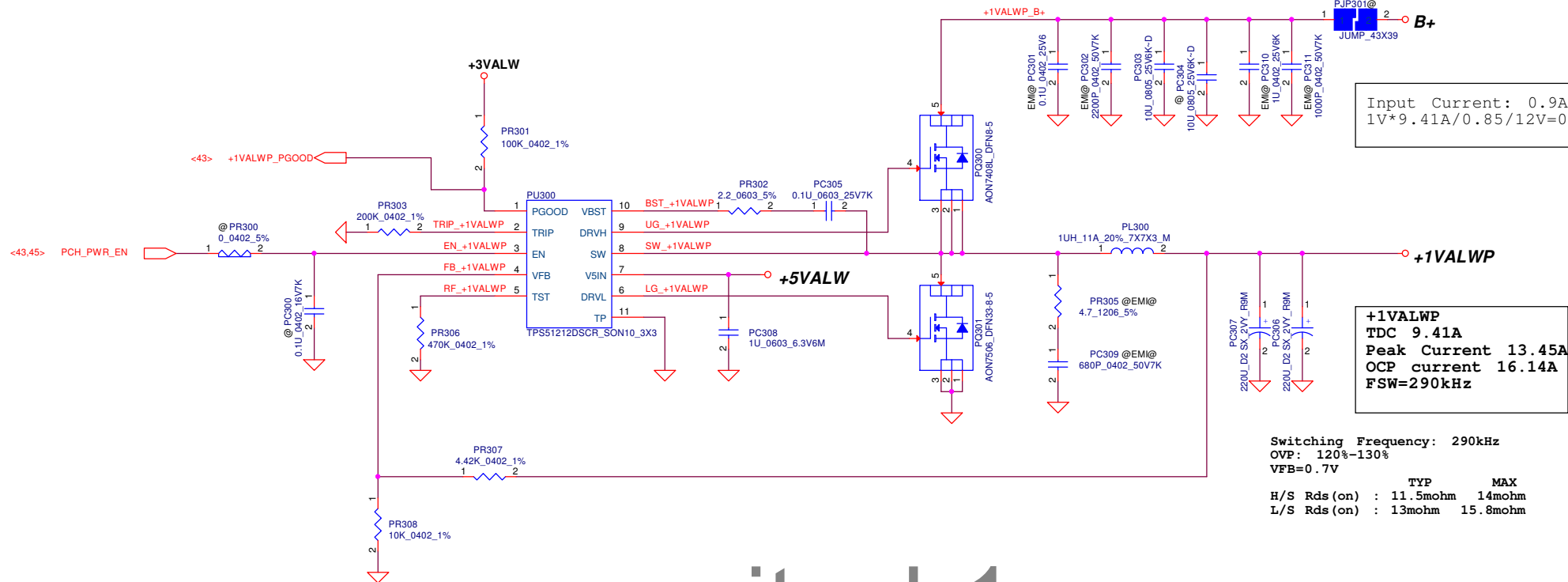
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Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title		
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				Size	Document Number	Rev
				LA-D751P		
				Date:	Tuesday, August 16, 2016	Sheet 64 of 82



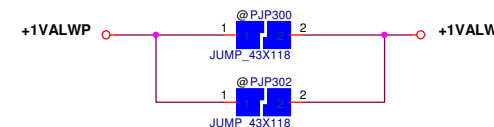
+2.5V_MEM
 TDC 0.63A
 Peak Current 0.9A
 OCP Current 3.5A

$$V_{out} = 0.8V * (1 + R_{up}/R_{down})$$

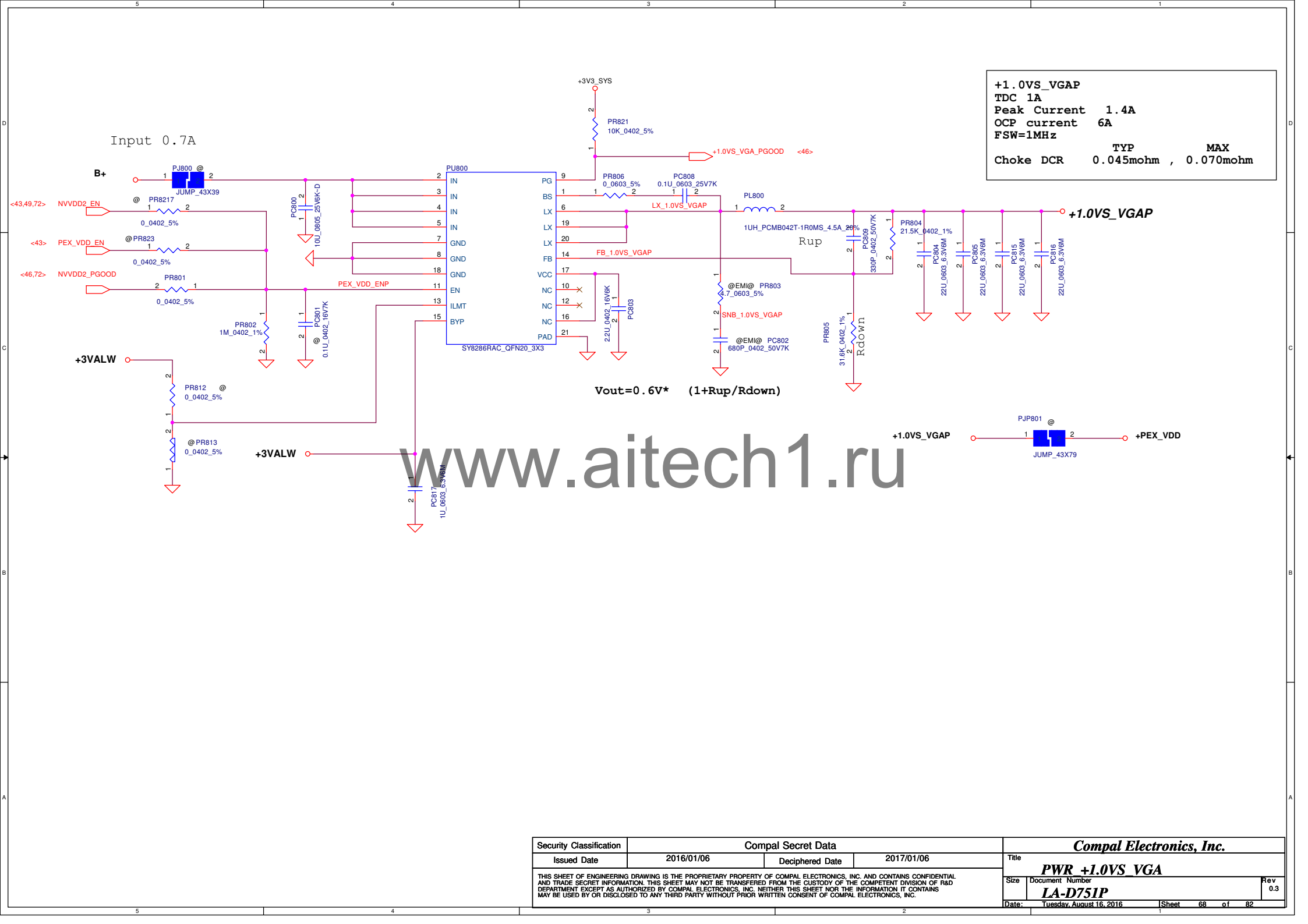
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2016/01/06		Deciphered Date		2017/01/06		Title	
										PWR +2.5V MEM	
										LA-D751P	
										Rev 0.3	
										Date: Tuesday, August 16, 2016	
										Sheet 65 of 82	



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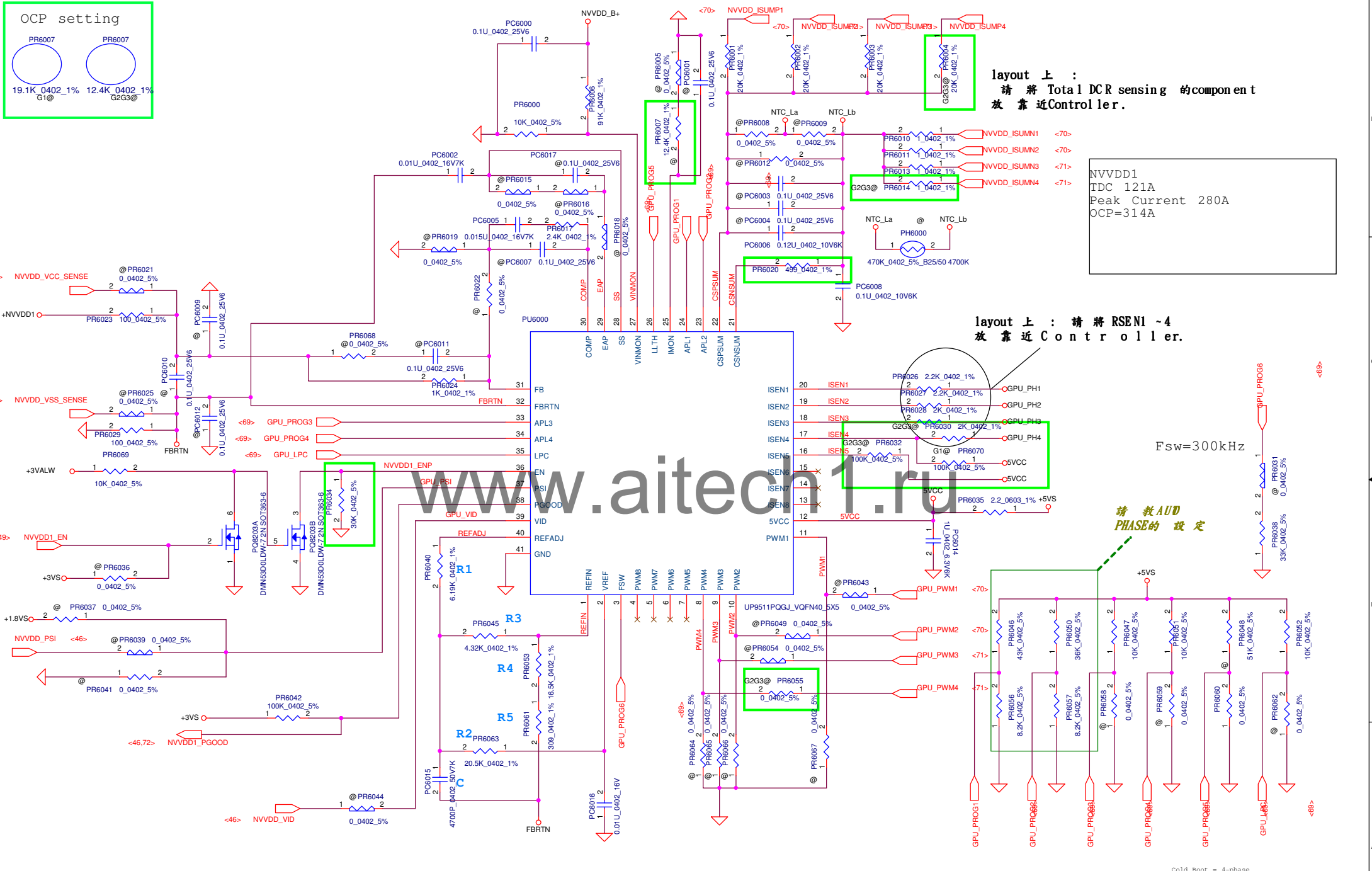
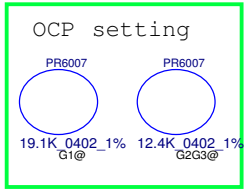
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	PWR +1VALWP
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+1.0VS_VGAP
TDC 1A
Peak Current 1.4A
OCP current 6A
FSW=1MHz
Choke DCR 0.045mohm , 0.070mohm
TYP MAX

$V_{out}=0.6V* (1+R_{up}/R_{down})$

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layout 上：
請將 Total DCR sensing 的 component
放靠近 Controller.

NVVDD1
TDC 121A
Peak Current 280A
OCP=314A

layout 上：請將 RSEN1~4
放靠近 Controller.

Fsw=300kHz

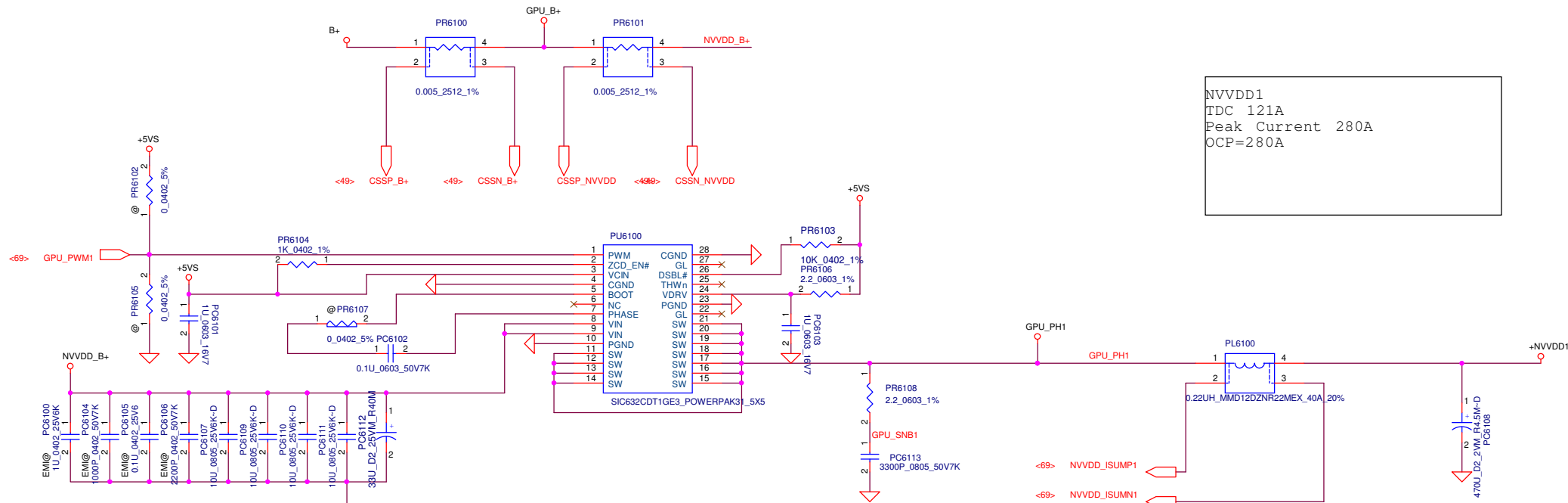
請教 AUD
PHASE 的設定

PWMVID 的 RC BOM
請根據 GPU's config
設定

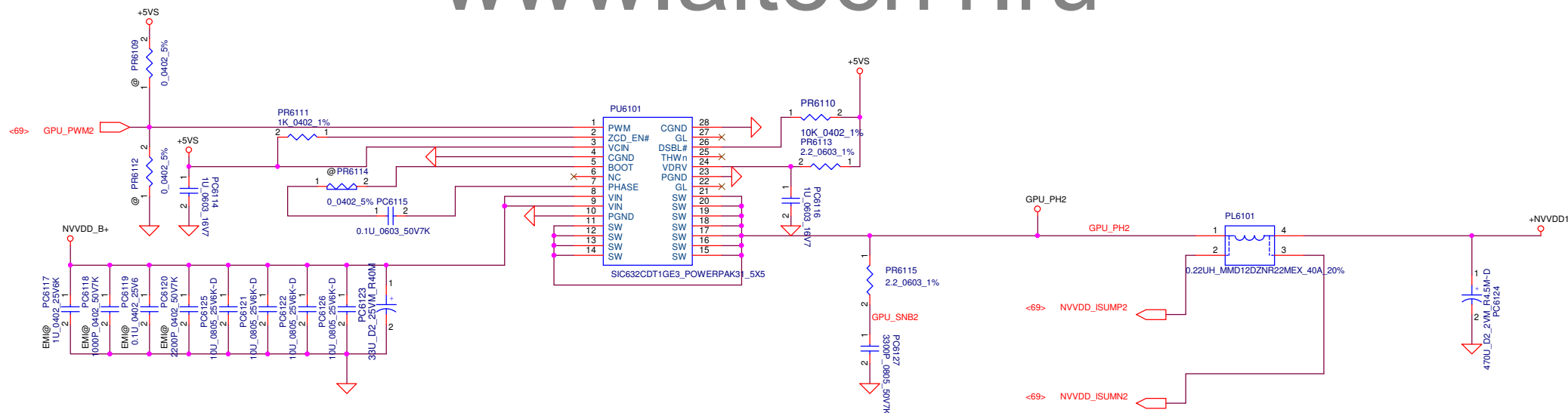
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2016/01/06		Deciphered Date		2017/01/06		Title			
								PWR VGA UP9511P			
								Size			
								Document Number			
								LA-D751P			
								Rev			
								0.3			
								Date			
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								69 of 82			

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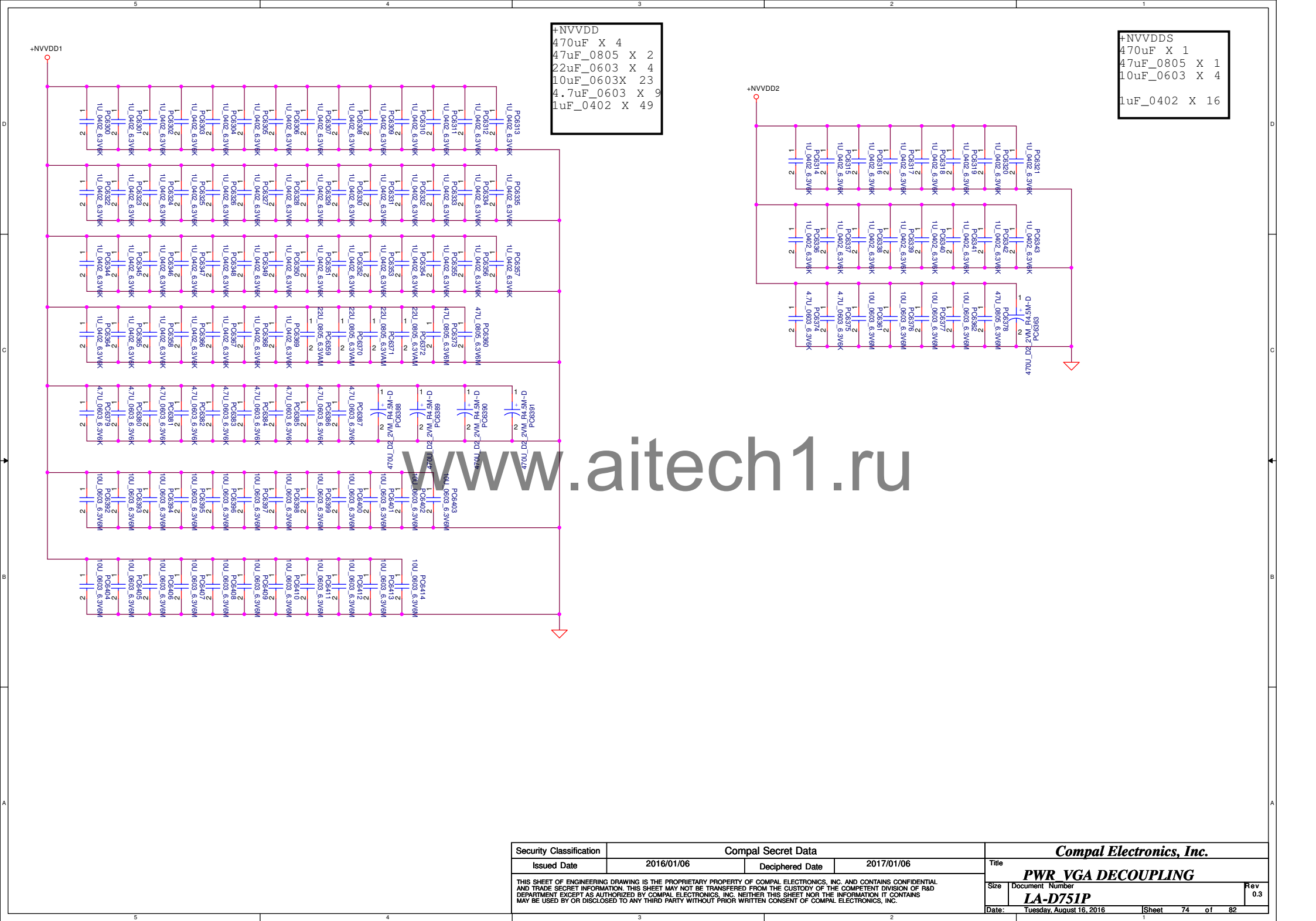
Cold Boot = 4-phase
Warm Boot = 4-phase



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+NVVDD
470uF X 4
47uF_0805 X 2
22uF_0603 X 4
10uF_0603X 23
4.7uF_0603 X 9
1uF_0402 X 49

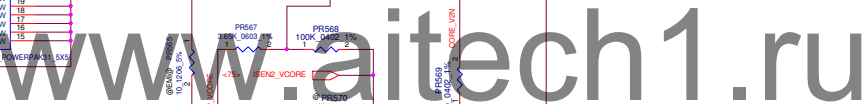
+NVVDD5
470uF X 1
47uF_0805 X 1
10uF_0603 X 4
1uF_0402 X 16

Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		PWR VGA DECOUPLING	
2016/01/06		2017/01/06		LA-D751P	
Size		Document Number		Rev	
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				82	



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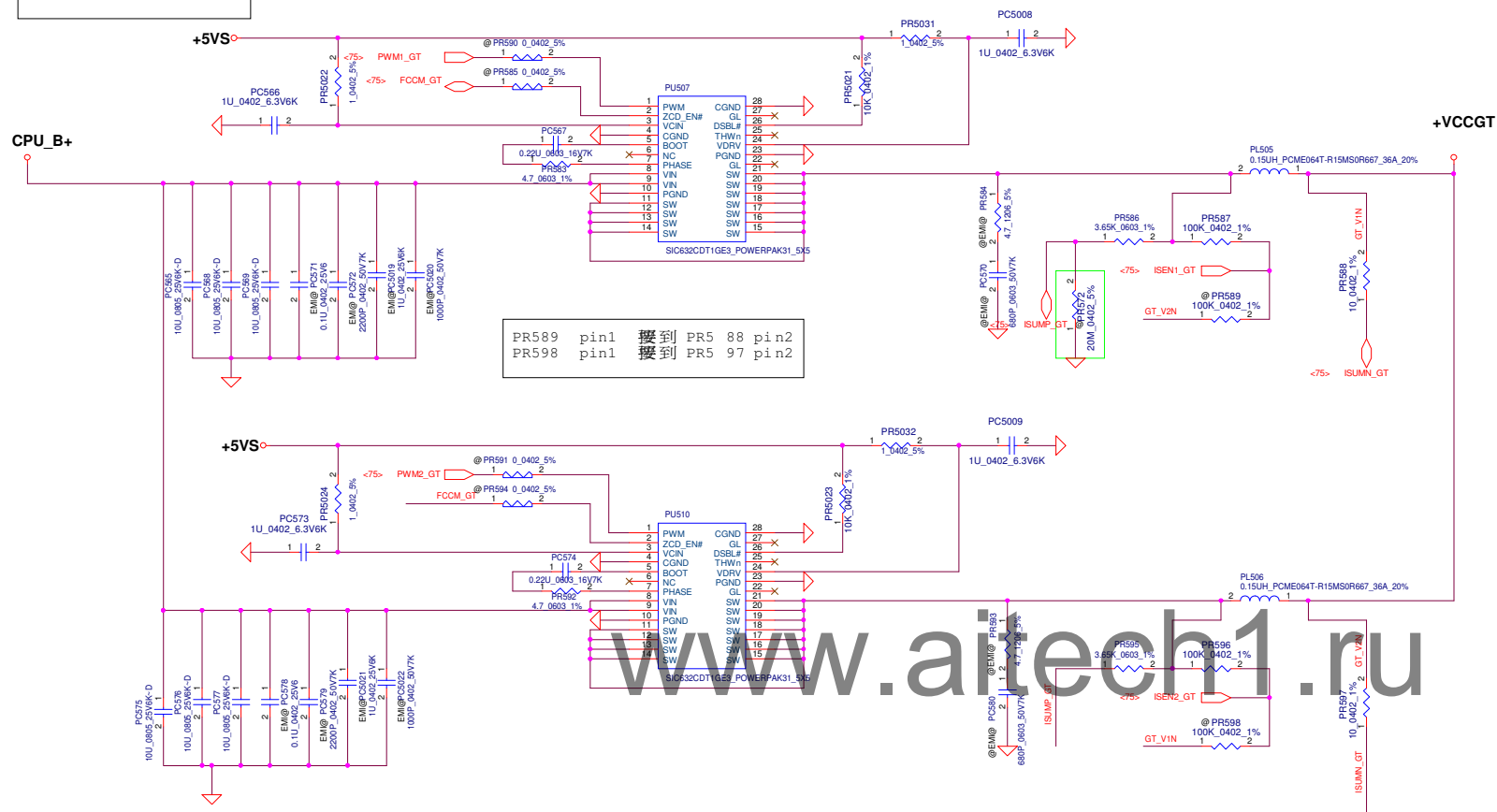
```
+VCC_CORE
TDC PL2 :56A
Peak Current 68A
OCP Current 81.6A
DCR 0.66mohm +/-7%
Load Line 1.8mV/A
```



Security Classification	Compal Secret Data		Title		Compal Electronics, Inc.	
Issued Date	2016/01/06	Declassified Date	2017/01/06	Size	Document Name	Rev
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<p>ALL INFORMATION CONTAINED HEREIN IS UNCLASSIFIED EXCEPT WHERE SHOWN OTHERWISE. THIS SET MAY NOT BE REPRODUCED OR THE CONTENTS COPIED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS WITHOUT THE WRITTEN PERMISSION OF COMPAL ELECTRONICS, INC.</p>				<p>Date: Tuesday, August 16, 2016 Sheet 76 of 82</p>		

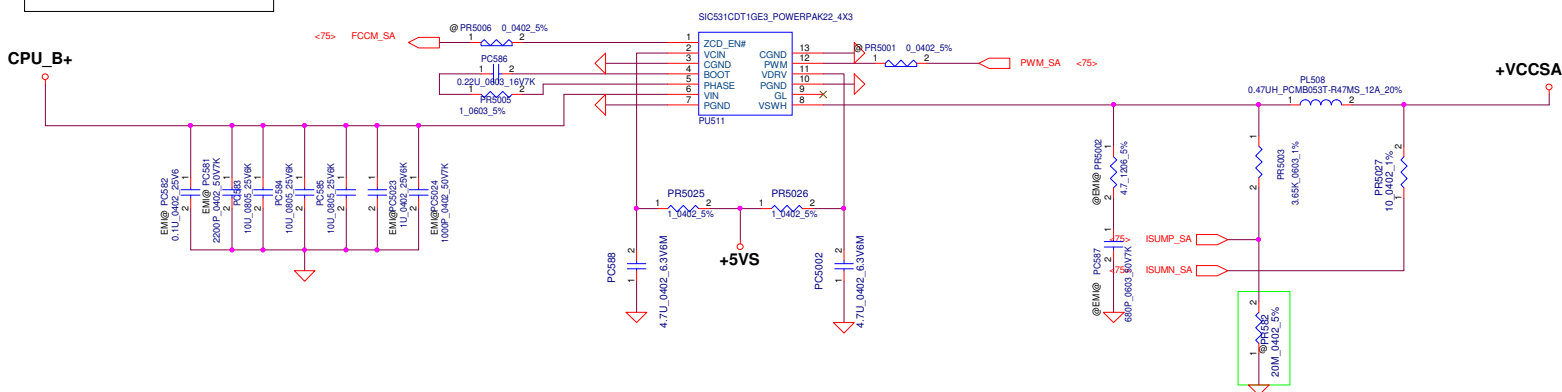
Input Current: 5.7A
 $1.5V \times 39A / 0.85 / 12V = 5.7$

```
+VCC_GT
TDC PL2 :39A
Peak Current 54A
OCP Current 64.8A
DCR 0.66mohm +/-7%
Load Line 2.65mV/A
```



```
+VCC_SA
TDC PL2 :10A
Peak Current 11A
OCP Current 13.2A
DCR 7.4mohm typ
Load Line 9.1mV/A
```

Input Current: 1.0A
 $1.05V \cdot 10A / 0.85 / 12V = 1.0$



Security Classification		Compal Secret Data		Compal Electronics, Inc. PWR VCORE +VCCGT,+VCCSA	
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+VCC_CORE

+VCCGT

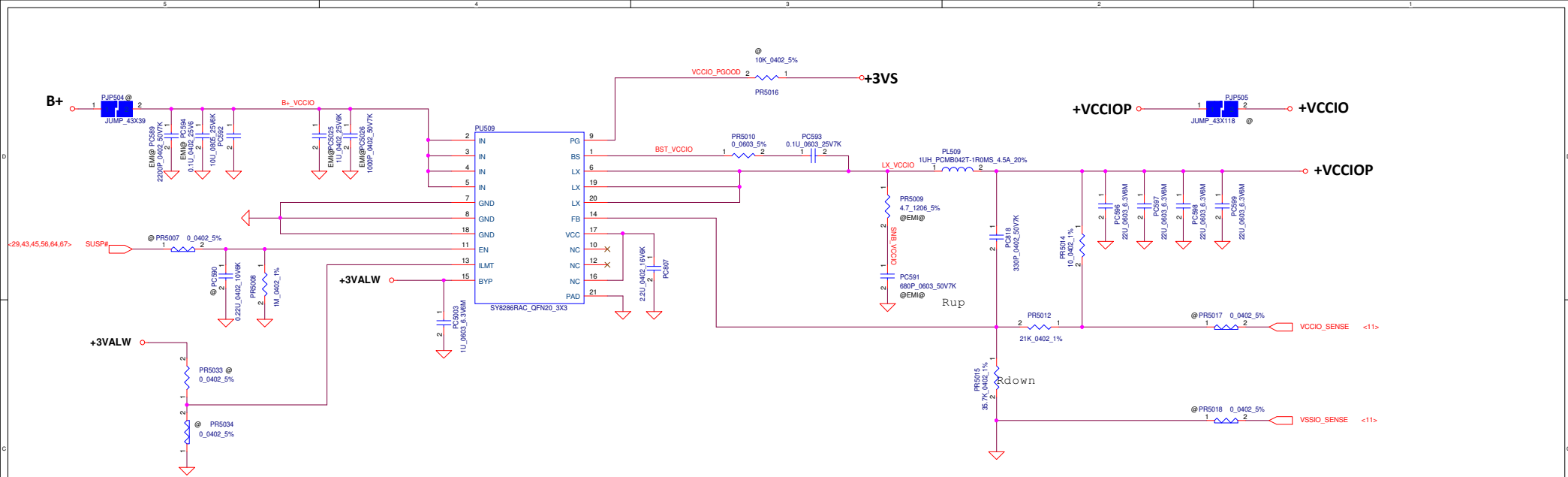
+VCCSA

VCC_CORE			
220uF	X3		
47uF_0805	X	4	
22uF_0603	X	8	
10uF_0402	X	28	
1uF_0201	X	63	

VCC_GT			
220uF	X4		
47uF_0805	X	6	
22uF_0603	X	8	
10uF_0402	X	3	
1uF_0201	X	68	

VCC_SA			
220uF	X1		
47uF_0805	X	1	
10uF_0402	X	7	
1uF_0201	X	3	

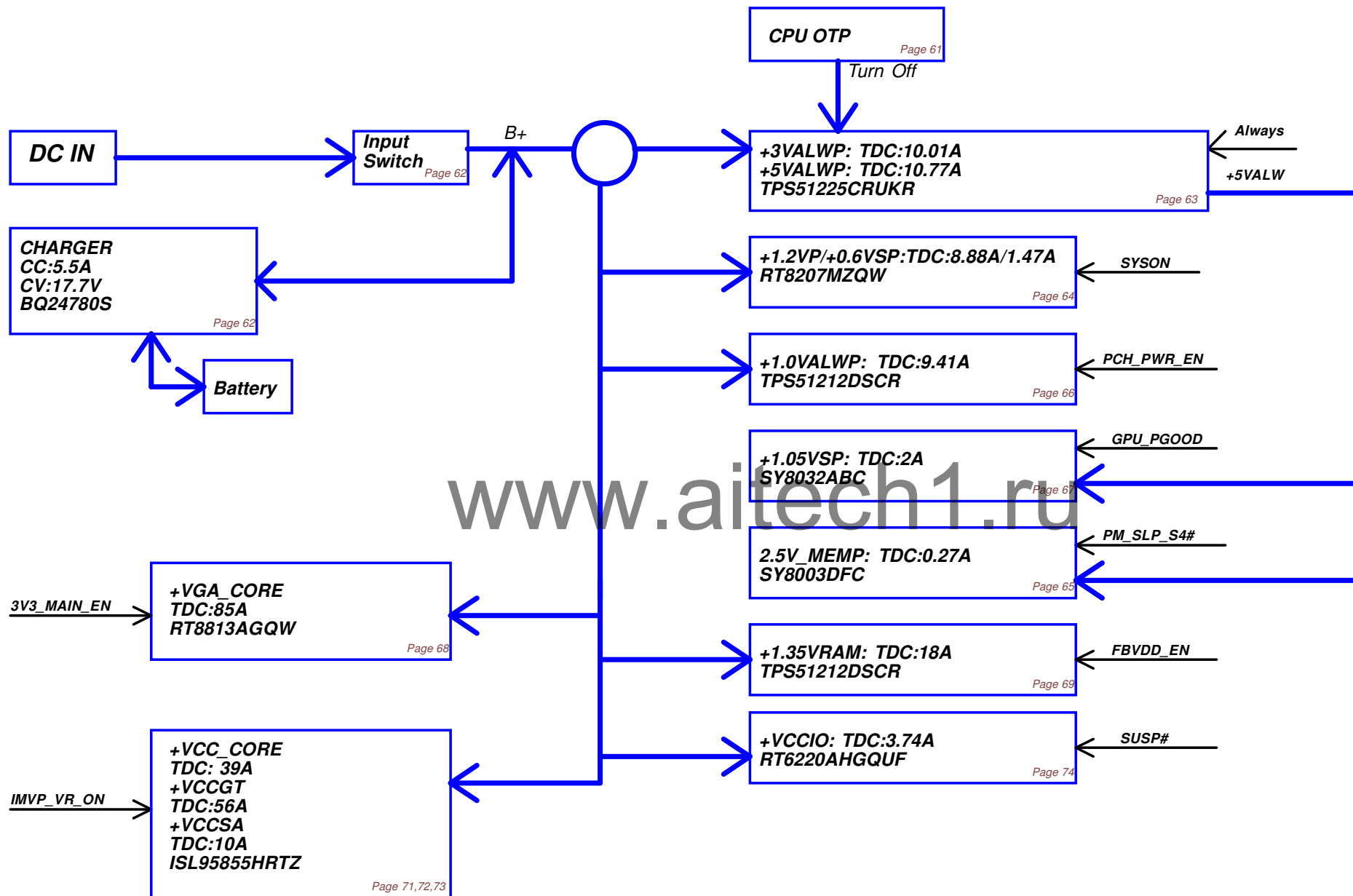
Security Classification		Compal Secret Data		Title	
Issued Date	2016/01/06	Deciphered Date	2017/01/06	PWR-CPU DECOUPLING	
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+VCCIO_P (0.95V)
TDC 3.85 A
Peak Current 5.5 A
OCP Current 6 A Fix by IC
TYP MAX
Choke DCR 24.0mohm , 27.0mohm

Power block



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Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	69	VGA_UP9511P	2016/03/28	Compal_PWR	For EE request to fine tune power sequence.	1. Change PR6020 from 100 Ohm to 500 Ohm. 2. Change PR6007 from 5.1k Ohm to 13.3k Ohm	0.2
2	64	+1.2VP/+0.6VSP	2016/03/28	Compal_PWR	Add component for XMP	1. Change PR213 from 20k Ohm to 60.4k Ohm.	0.2
3	69	VGA_UP9511P	2016/03/30	Compal_PWR	For EE request to fine tune power sequence.	1. Change PR6069&PR6036 pin 1 from +3V3_SYS to +3VALW .	0.2
4	69	VGA_UP9511P	2016/04/01	Compal_PWR	For EE request to fine tune power sequence.	1. Change PR6033 connect to NVVDD_EN.	0.2
5	72	+NVVDD2	2016/04/01	Compal_PWR	For EE request to fine tune power sequence.	1. Change PR6402 connect to NVVDD_EN.	0.2
6	73	+1.35VS_VGAP	2016/04/11	Compal_PWR	For NV request.	1. Change +3VS to +1.8V_AON	0.2
7	64	+1.2VP/+0.6VSP	2016/04/11	Compal_PWR	Add component for XMP	1. Add PR212 to 1k Ohm. 2. Add PC217 to 0.1uF. 3. Add PQ202 MOS.	0.2
8	73	+1.35VS_VGAP	2016/04/11	Compal_PWR	For BOM control	1. Add PR8211 of 34.8k Ohm for SAMSUNG@ 2. Add PR8211 of 30k Ohm for MIRCON@ 3. Add PR8215 of 52.3k Ohm for SAMSUNG@ 4. Add PR8215 of 68.1k Ohm for MIRCON@ .	0.2
9	68	+1VS_VGAP	2016/04/11	Compal_PWR	For +1VS_VGAP OCP setting.	1. Change PL800 from 1UH_MAMK2520T1R0M_3.1A to 1UH_PCMB042T-1R0MS_4.5A.	0.2

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
10	75	VCORE_ISL95829	2016/05/18	Compal_PWR	For CPU_VCORE setting.	1. Change PC507 from 680pF to 1000pF. 2. Change PC517 from 0.047uF to 0.068uF. 3. Change PR548 from 95.3kohm to 105kohm.	0.3
11	62	CHARGER	2016/05/18	Compal_PWR	For CHARGER ILIM setting.	1. Change PR710 from 2kohm to 5.11kohm. 2. Change PR711 from 2.43kohm to 3.16kohm.	0.3
12	68	+1.0VS_VGAP	2016/05/18	Compal_PWR	Add component for +1.0VS_VGAP_EN	1. Add PR801 for 0ohm.	0.3
13	69	VGA_UP9511P	2016/05/18	Compal_PWR	For VGA_UP9511P_EN	1. Change PQ8203 from TR DMN66D0LDW-7 2N SOT363-6 to TR DMN53D0LDW-7 2N SOT363-6.	0.3
14	73	+1.55VRAM	2016/06/20	Compal_PWR	Add component for +1.55VRAM	1. Add PR8219 or 0ohm.	0.4
15	62	CHARGER	2016/06/20	Compal_PWR	For charger setting.	1. Add PQ701, PQ702, PQ707, PQ708, PQ703 of AON7506_DFN33-8-5 for X760	0.4

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